June 6, 2012

Variation-Tolerant Design of Analog CMOS Circuits – Lecture 2

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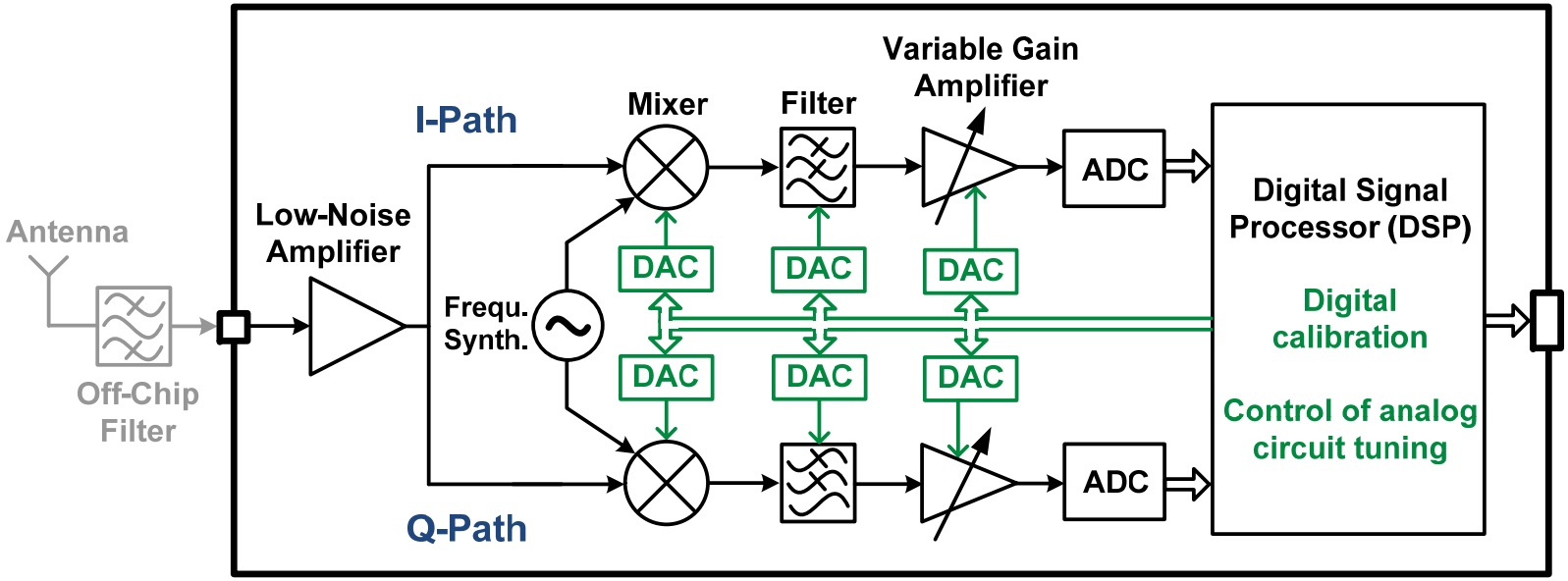
Short Course held at:

Universitat Politècnica de Catalunya
Barcelona, Spain

Outline – Lecture 2

- Digitally-assisted analog circuit design & performance tuning
  - LNAs
  - Mixers
  - Filters
  - Example: subthreshold LNA design techniques
- Case study: Digitally-assisted linearization of operational transconductance amplifiers
- Case study: Variation-aware continuous-time ΔΣ analog-to-digital converter design

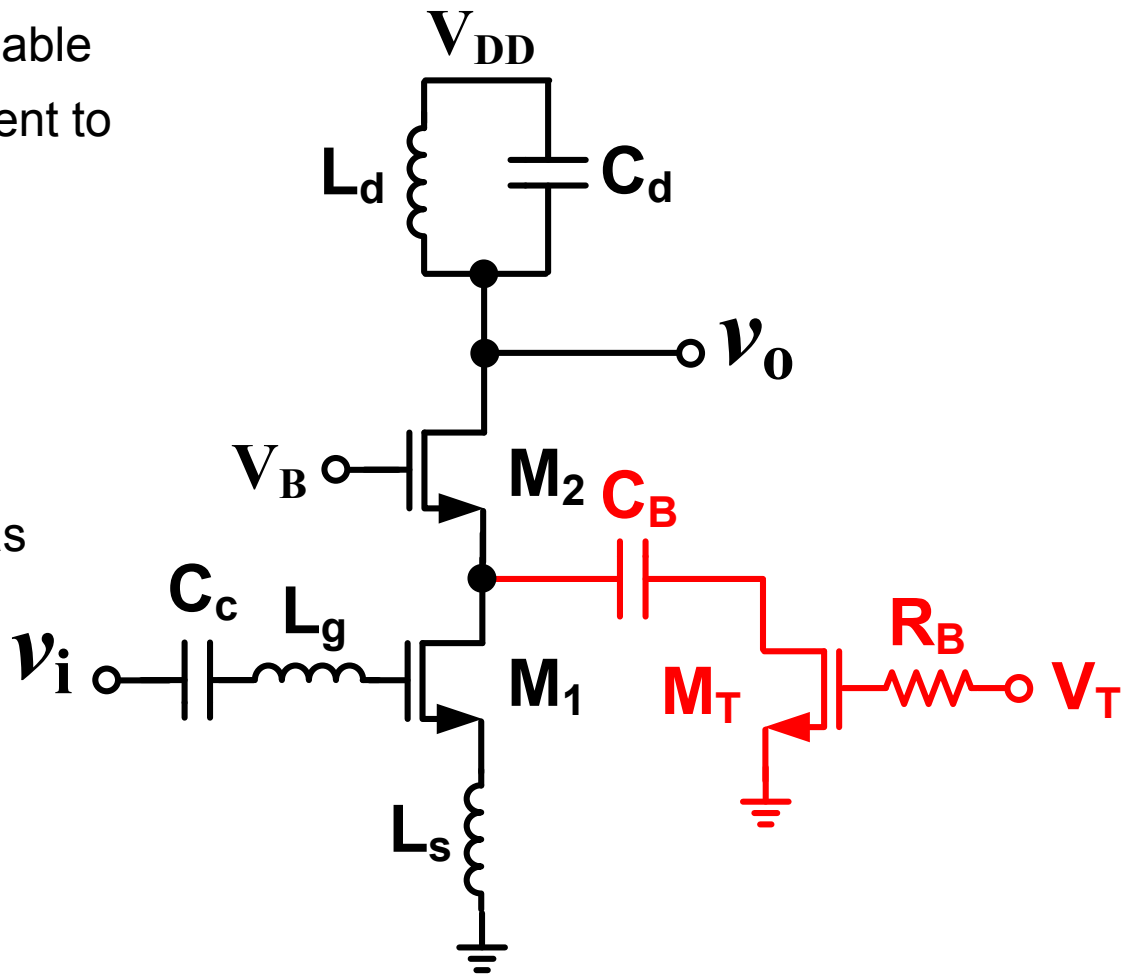
Example Application: Digitally-Assisted Analog Blocks



- Digitally-assisted receiver calibration
  - Analog tuning with digital-to-analog converters (DACs)
  - Digital correction and control
  - Requires programmable analog circuits for performance tuning

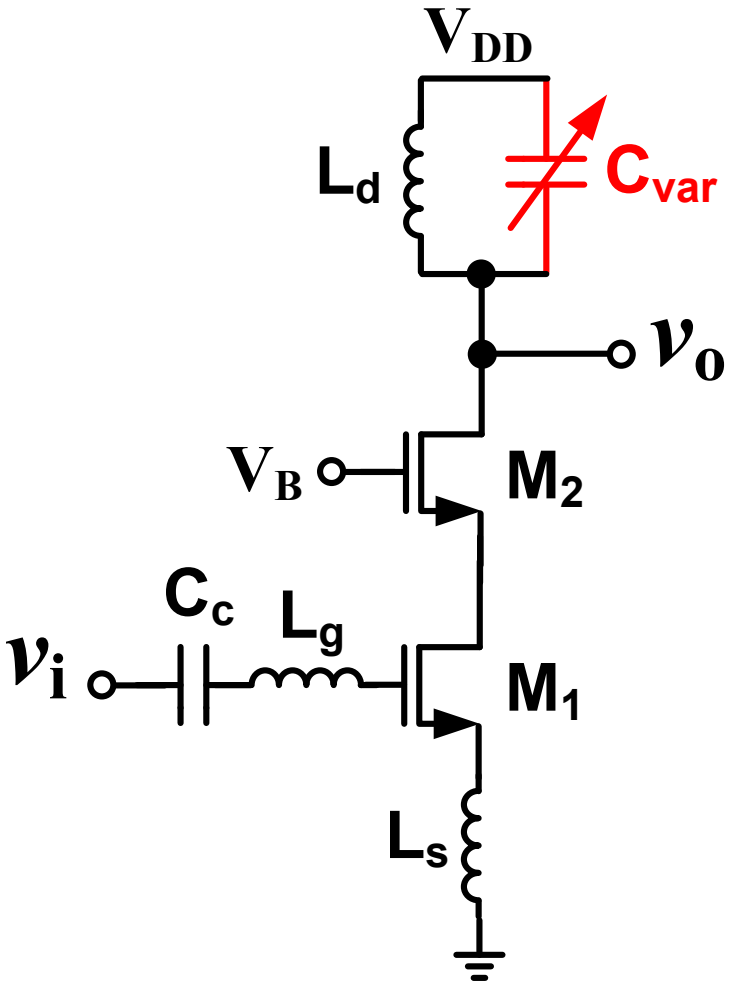
LNA Gain Tuning Example

- Auxiliary transistor M_T (variable resistor) diverts signal current to the AC ground
  → Gain control
  (range: 3.6-12.5dB)
- C_B ensures that the DC bias remains unaffected
- Linearity could be affected



C.-H.Liao and H.-R. Chuang, "A 5.7-GHz 0.18-μm CMOS gain-controlled differential LNA with current reuse for WLAN receiver," *IEEE Microwave and Wireless Components Letters*, vol. 13, no. 12, pp.526-528, Dec. 2003.

LNA Center Frequency Tuning Example



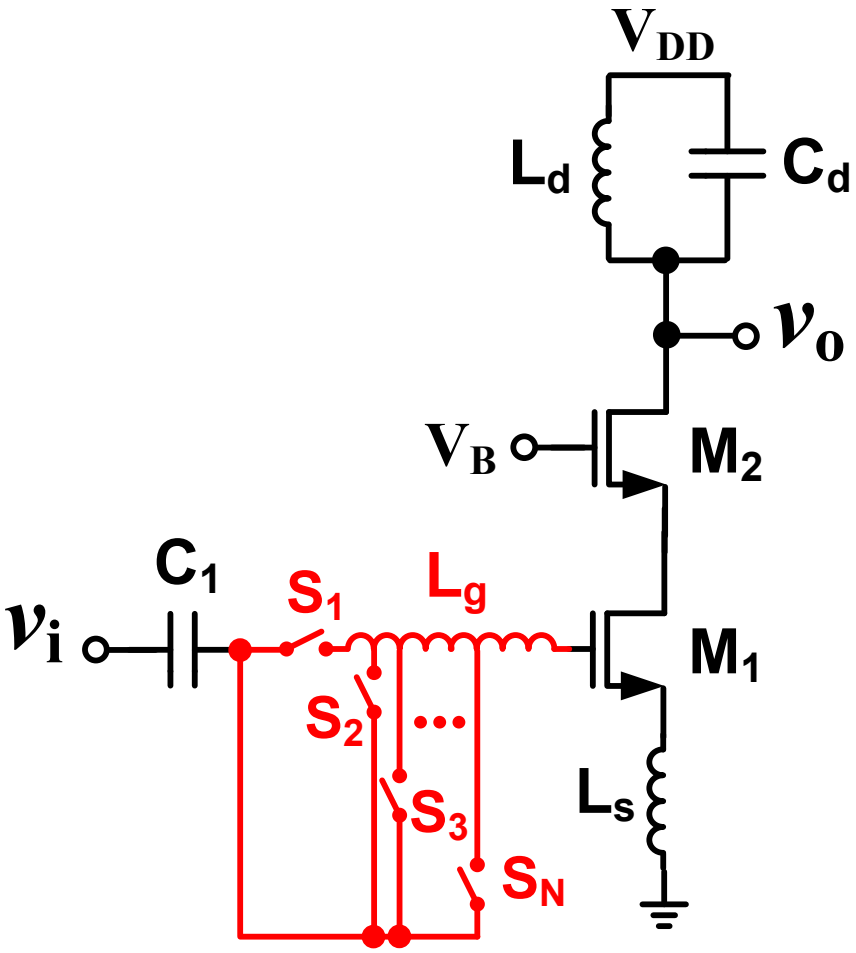
- Example application: WLAN (2.4GHz, 5GHz)

- 4-bit resolution for C_{var}

  → <0.4dB gain error due to center frequency shift from process variations

N. Ahsan, J. Dabrowski, and A. Ouacha, "A self-tuning technique for optimization of dual band LNA, " in *Proc. European Conf. on Wireless Technology (EuWiT)*, Jan. 2009, pp.178-181.

LNA Impedance Matching Tuning

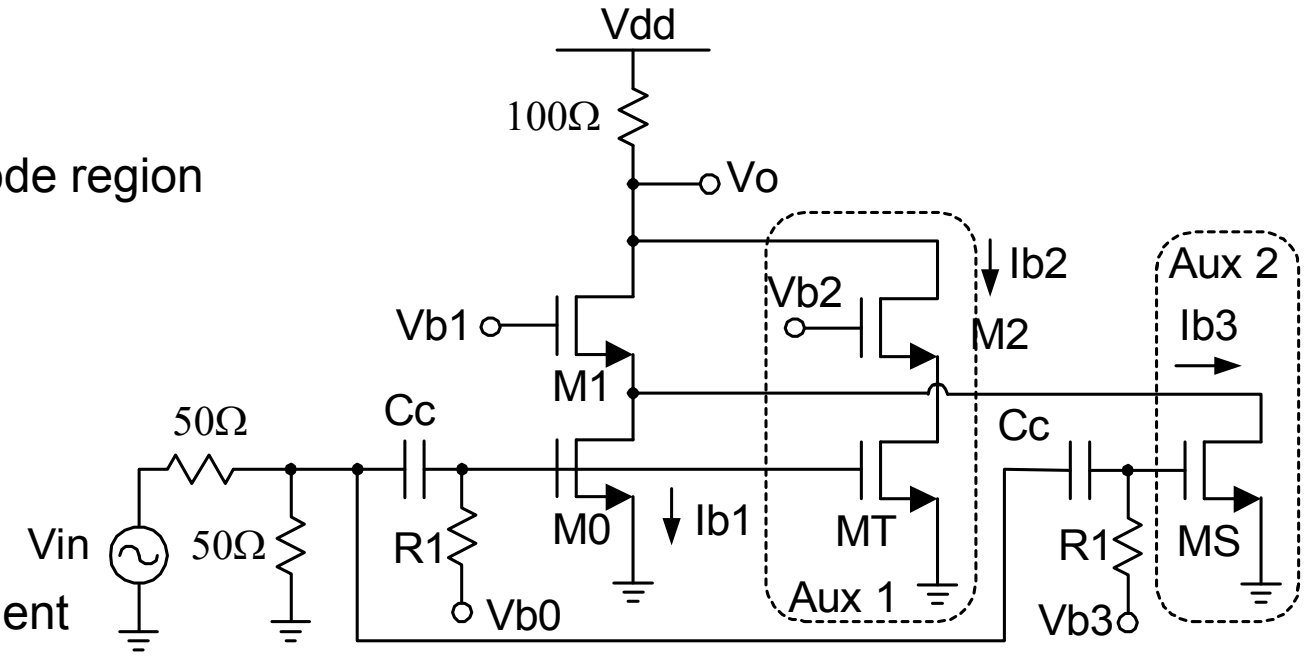


- S_{11} tuning
  - L_g is tapped at 5 points in the outermost turn
  - Control: switches S_1-S_N
- With automatic cal. loop
  - Aux. amplifier, peak detector, digital logic
  - Converges within 30μs
- ~0.4dB lower NF (due to switches)

T. Das, A. Gopalan, C. Washburn, and P. R. Mukund, "Self-calibration of input-match in RF front-end circuitry," *IEEE Trans. Circuits and Systems II: Express Briefs*, vol. 52, no. 12, pp. 821-825, Dec. 2005.

LNA Linearity

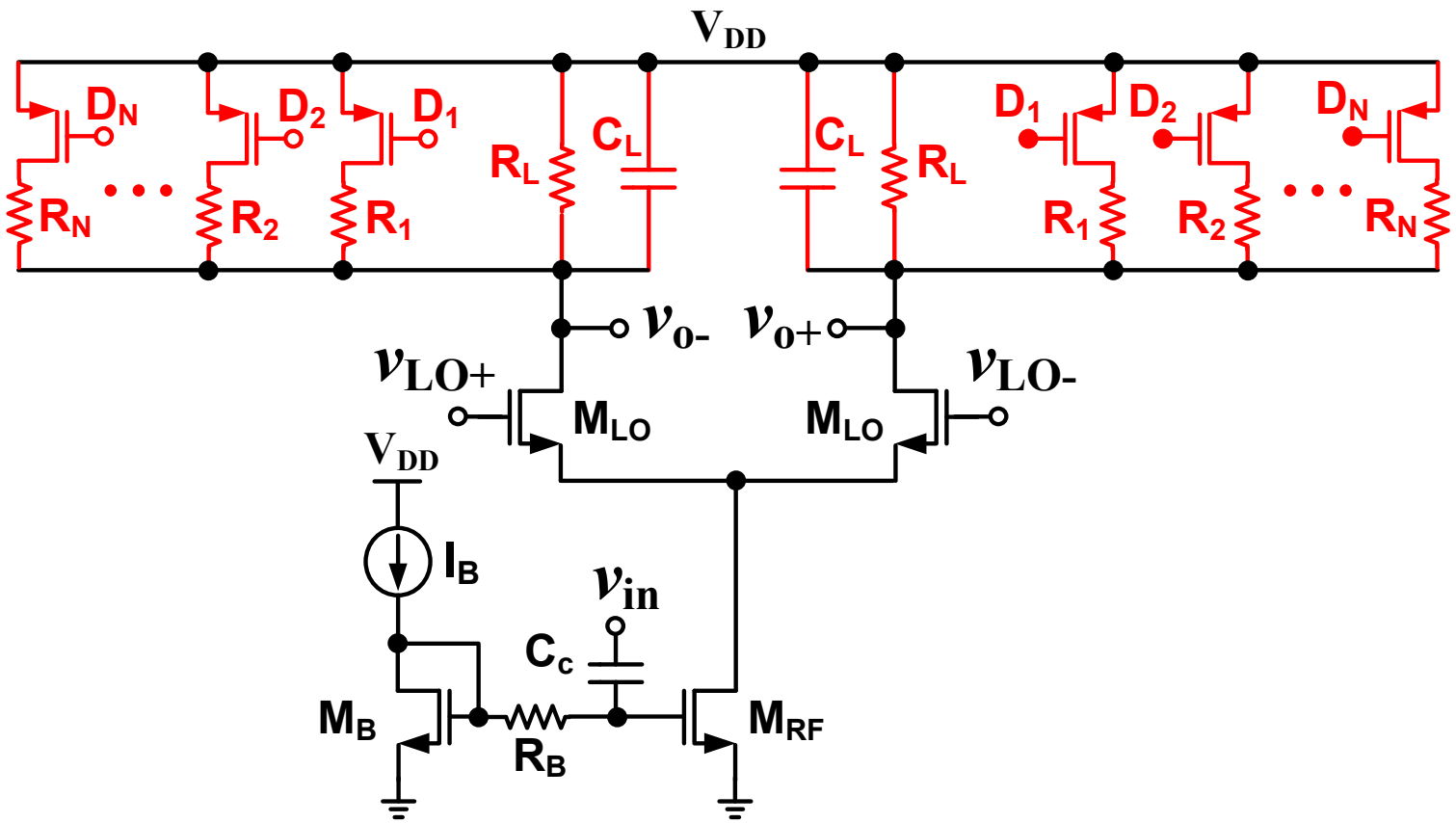
- Linearity Tuning
  - MT Operates in triode region
  - MS is biased in subthreshold
  - Non-linearities of the main transistor M0 are canceled
- >10dB IM3 improvement



- With tuning knobs
  - LNA linearity could be monitored in DSP or through power detectors
  - More robust against PVT variations
- NF increases <0.25dB and power increases by 5%

M. Geddada, J. Won-Park, and J. Silva-Martinez "Robust Derivative superposition Method for Linearizing Broadband LNAs," *IEE Electronics Letters, Vol. 45, pp. 435-436, April 2009*.

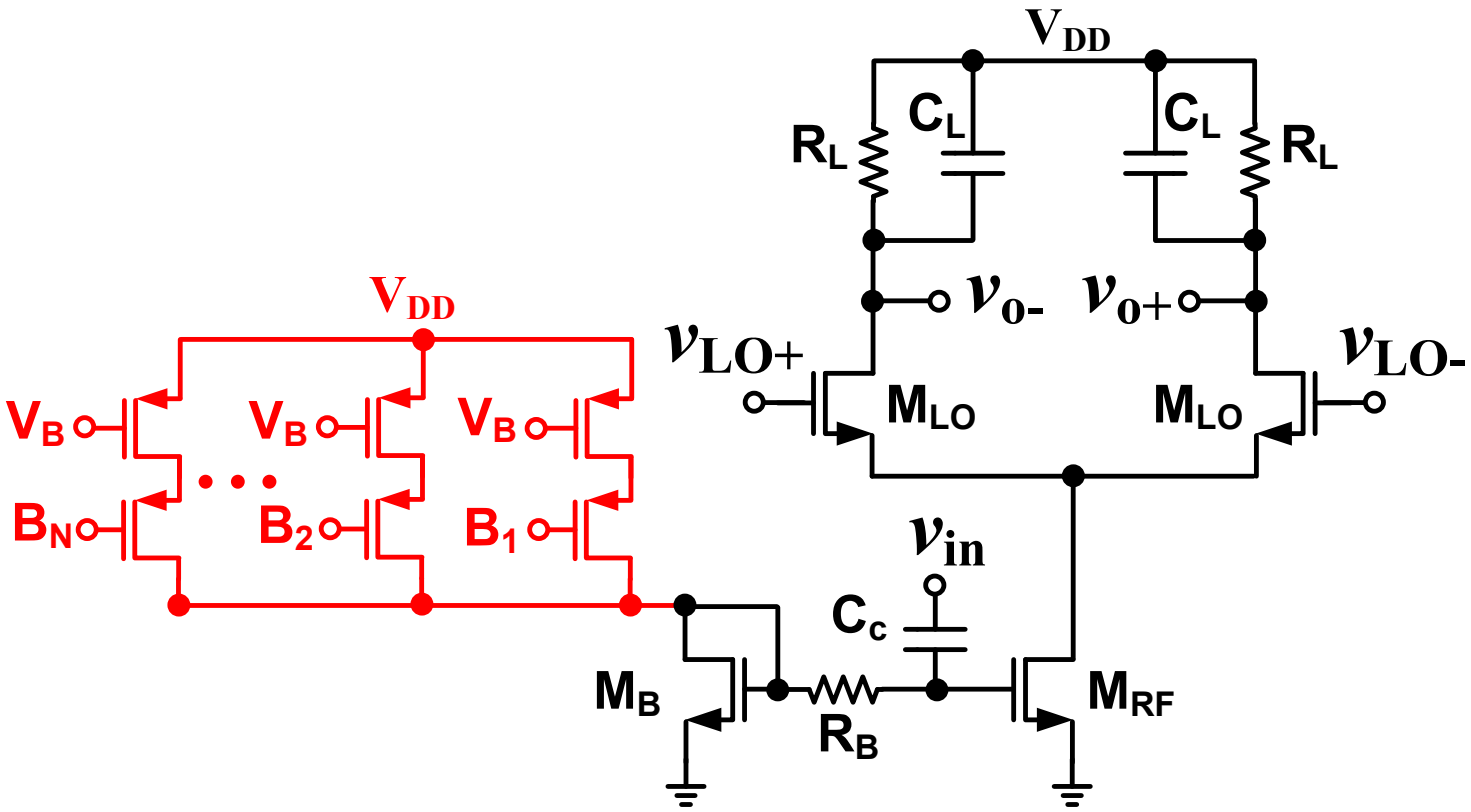
Mixer IIP2 Tuning Example



- 5-bit load resistor control with switches D_1-D_N
- Reduced 2nd-order non-linearities due to mismatches
- +60dBm IIP2 (>20dB improvement)

K. Kivekas, A. Parssinen, J. Ryynanen, J. Jussila, and K. Halonen, "Calibration techniques of active BiCMOS mixers," *IEEE J. Solid-State Circuits*, vol. 37, no. 6, pp. 766-769, Jun 2002.

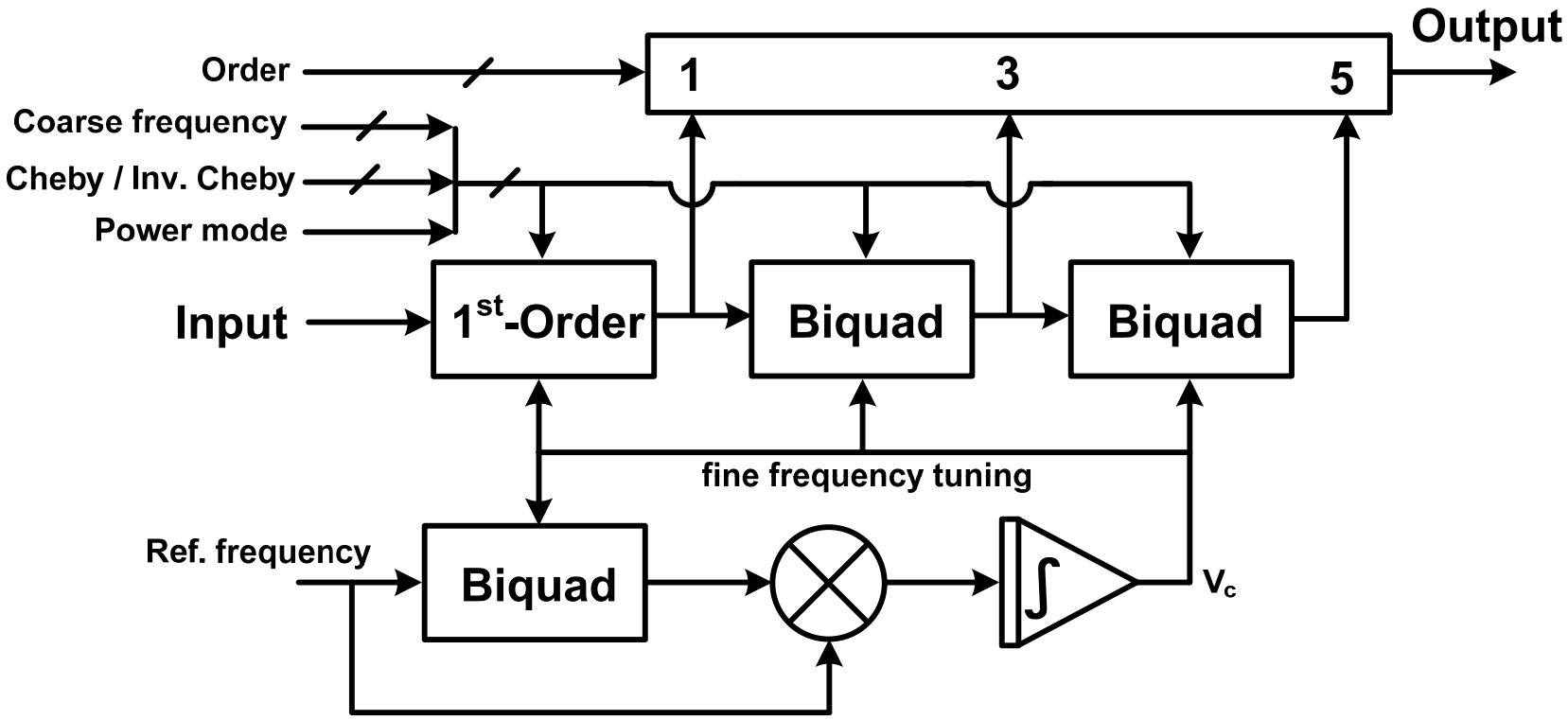
Mixer Gain Tuning Example



- 4-bit bias current control with switches B_1-B_N
- Less I/Q gain error: 0.1-0.2dB → 0.05dB ($\Delta\theta_{I/Q}$<3.5°)
- 1.5dB gain tuning range (steps = 0.09-0.13dB)

K. Kivekas, A. Parssinen, J. Ryynanen, J. Jussila, and K. Halonen, "Calibration techniques of active BiCMOS mixers," *IEEE J. Solid-State Circuits*, vol. 37, no. 6, pp. 766-769, Jun 2002.

Active-RC Filter Example

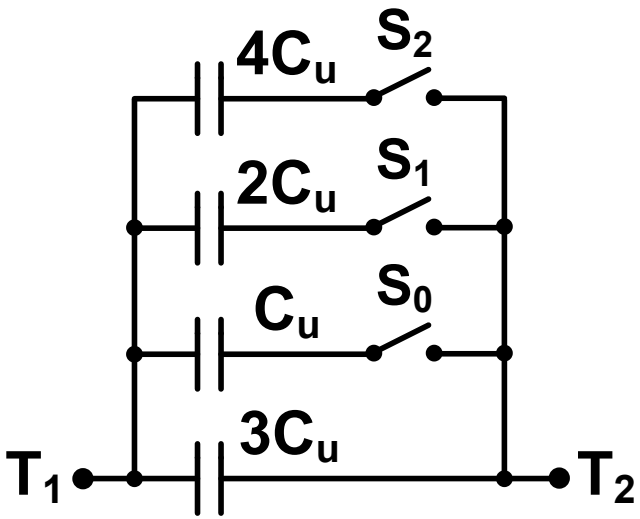


- Reconfigurable: Chebyshev/Inv. Chebyshev, order: 1,3,5
- Continuously tunable: 1-20MHz cutoff frequency
- Power-adjustable: 3-7.5mW

H. Amir-Aslanzadeh, E. J. Pankratz, and E. Sánchez-Sinencio, "A 1-V +31 dBm IIP3, reconfigurable, continuously tunable, power-adjustable active-RC LPF," *IEEE J. Solid-State Circuits*, vol. 44, no. 2, pp. 495-508, Feb. 2009.

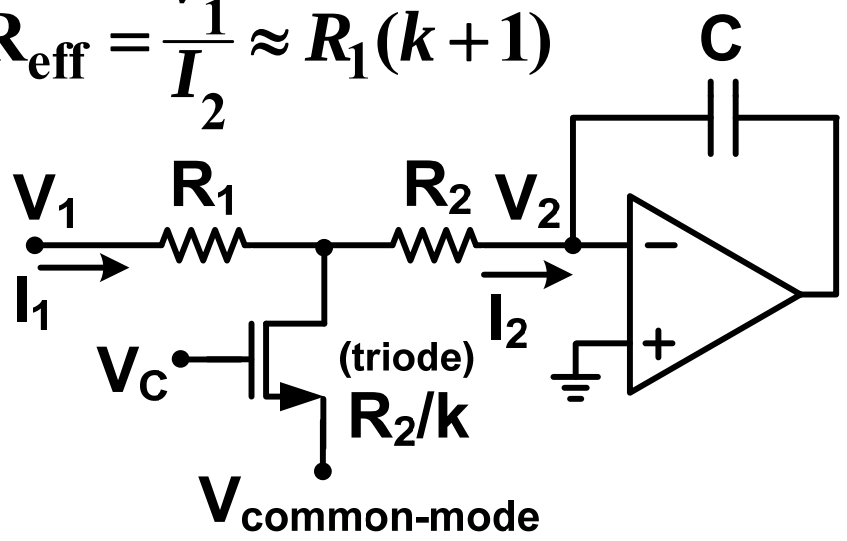
Active-RC Filter: Frequency Tuning

- Cutoff frequency tuning with adjustable elements in the filter sections



Coarse tuning with capacitors

$$R_{eff} = \frac{V_1}{I_2} \approx R_1(k+1)$$



Fine tuning with continuous impedance multipliers

H. Amir-Aslanzadeh, E. J. Pankratz, and E. Sánchez-Sinencio, "A 1-V +31 dBm IIP3, reconfigurable, continuously tunable, power-adjustable active-RC LPF," *IEEE J. Solid-State Circuits*, vol. 44, no. 2, pp. 495-508, Feb. 2009.

Subthreshold Low-Noise Amplifier Design Techniques

Chun-hsiang Chang
Marvin Onabajo

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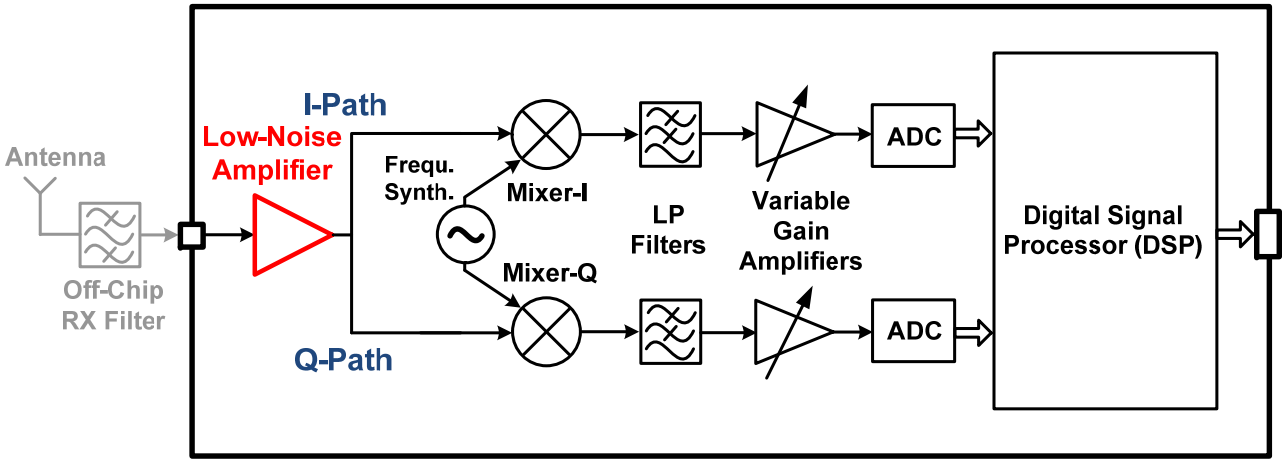
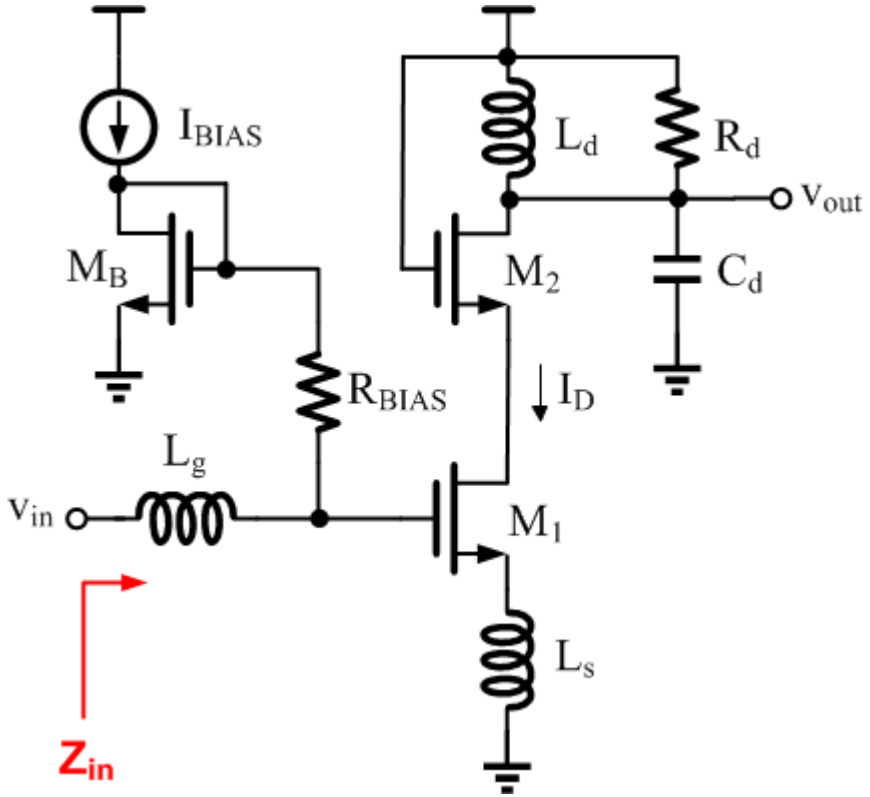
Low-Power Low-Noise Amplifier



- Motivation for biasing RF circuits in the subthreshold (weak inversion) region
  - High transition frequencies (f_t) of newer CMOS technologies enable subthreshold RF circuit design (< 3GHz) with sufficiently high transistor transconductance (gain)
  - **5-10 times less power consumption**
- Subthreshold design challenges
  - Degraded linearity & noise performance → for applications with relaxed requirements [wireless personal area network (WPAN), global positioning system (GPS), and wireless medical monitoring]
  - Larger devices → increased parasitic capacitances

Example: Input Impedance Matching

- Typical matching: $Z_{in} = 50\Omega$
  - $S_{11}(dB) = -\infty$ (ideal)
  - In practice: $-20dB < S_{11} < -10dB$



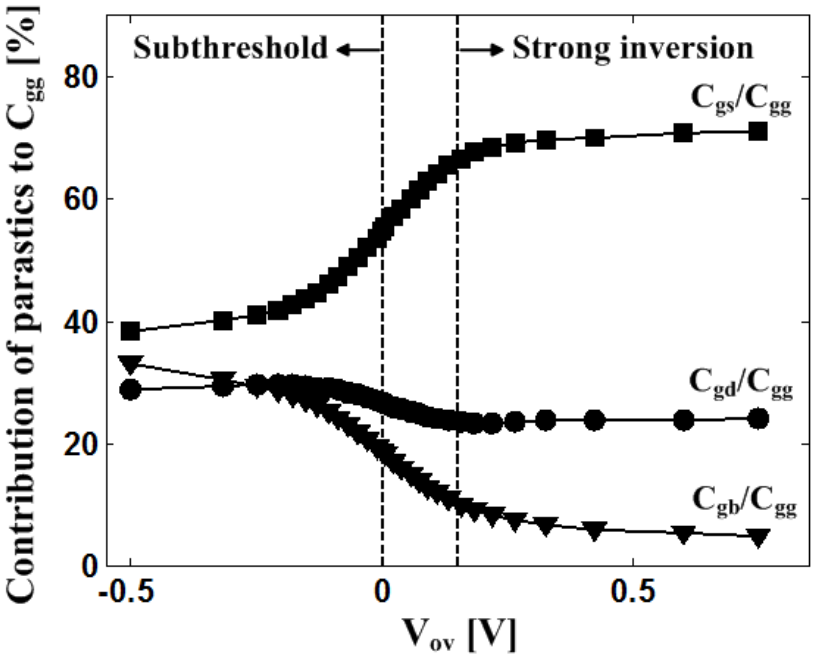
- Conventional approximation:

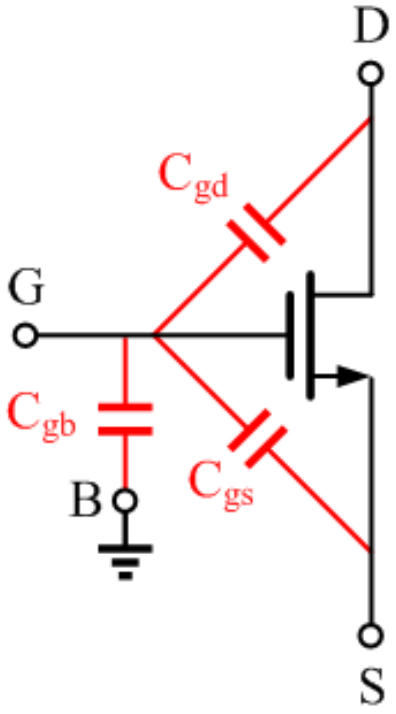
$$Z_{in} = L_s \frac{g_{m1}}{C_{gs1}} + j\left[\omega(L_s + L_g) - \frac{1}{\omega C_{gs1}}\right]$$

Issues with Subthreshold Biasing

- Larger parasitic capacitances
  - $C_{gg} = C_{gs} + C_{gd} + C_{gb}$
  - Inaccurate Z_{in} approximation with the conventional equation

- Different contributions to the total gate capacitance (C_{gg}):

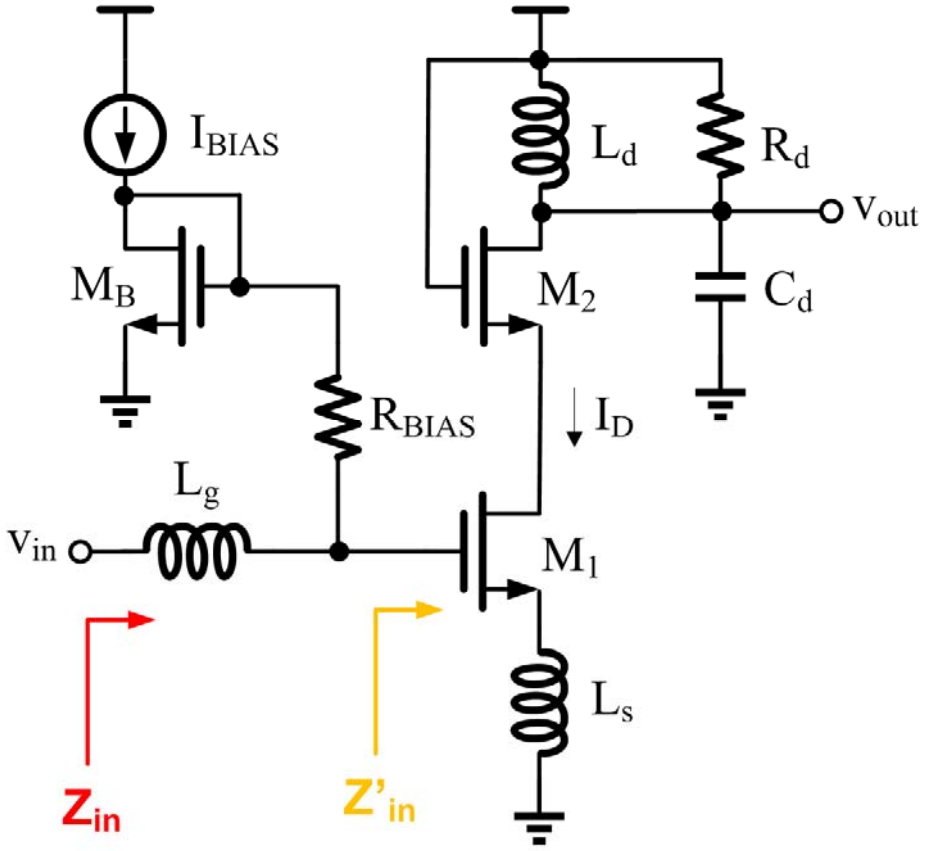




Improved Z_{in} Estimation

- Equations include the effects of C_{gs}, C_{gd}, C_{gb}
- Impact of M_2 (load) is considered
- Simplified calculations with a Matlab script

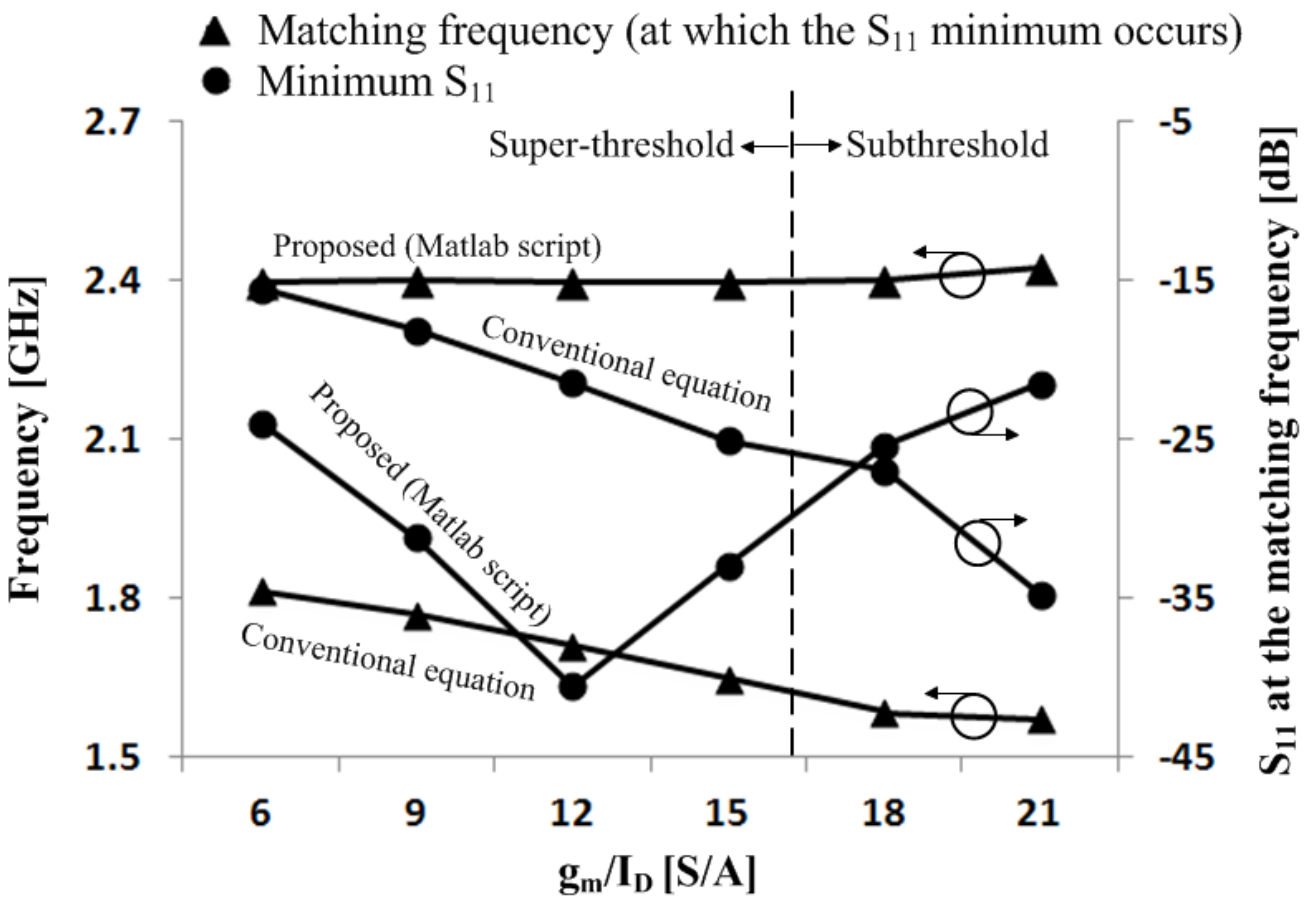
$$Z_{in} = sL_g + r_{g1} + Z_{in}' \,//\, \frac{1}{sC_{MF}}$$



where:
- r_{g1} is the small-signal gate resistance of M_1
- C_{MF} is the effective input Miller capacitance
- Z'_{in} is the impedance looking into the gate (without r_{g1}) → very long equation

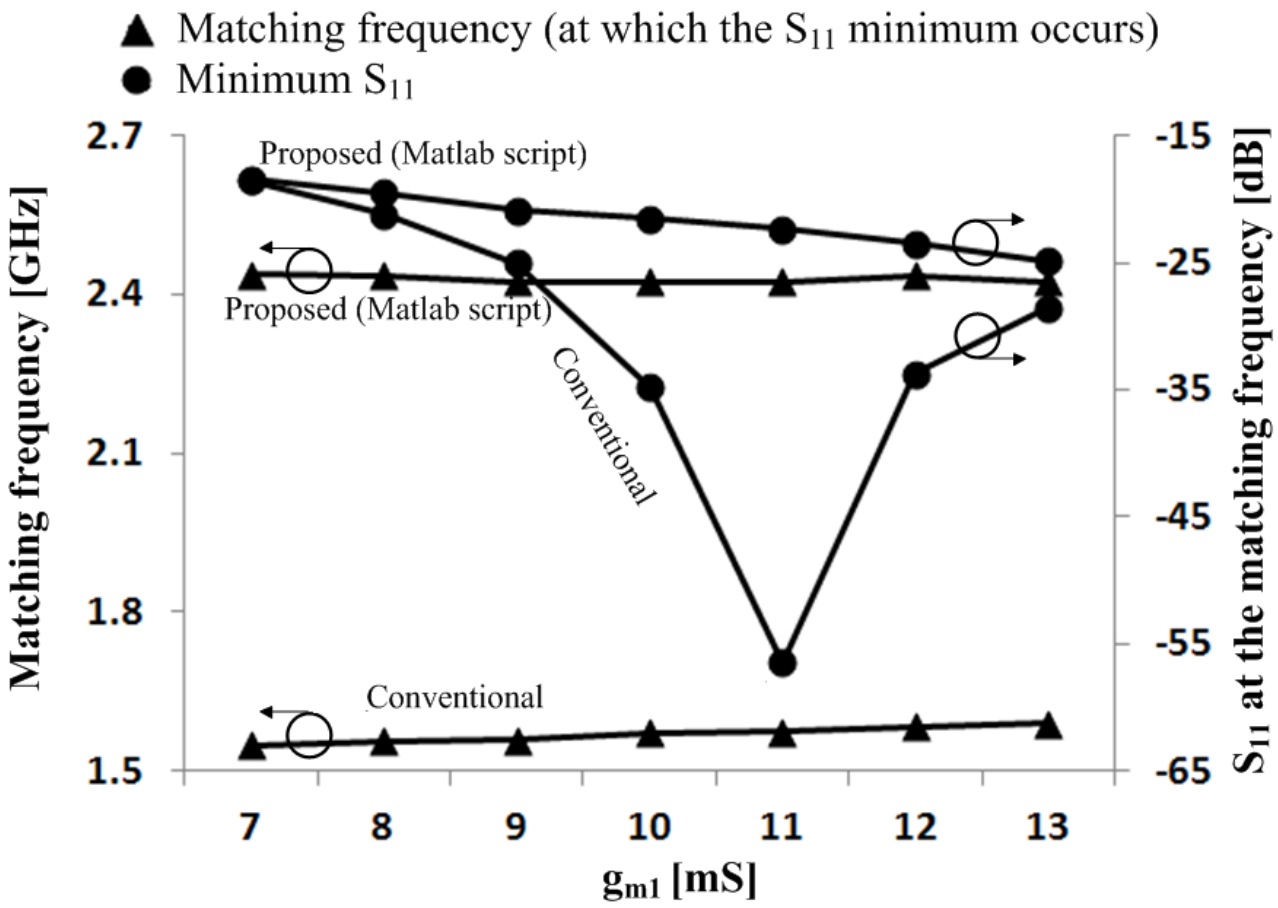
Simulation Results

- Desired matching frequency: 2.4 GHz
- 0.18 μm CMOS technology
- Comparison with different operating regions:



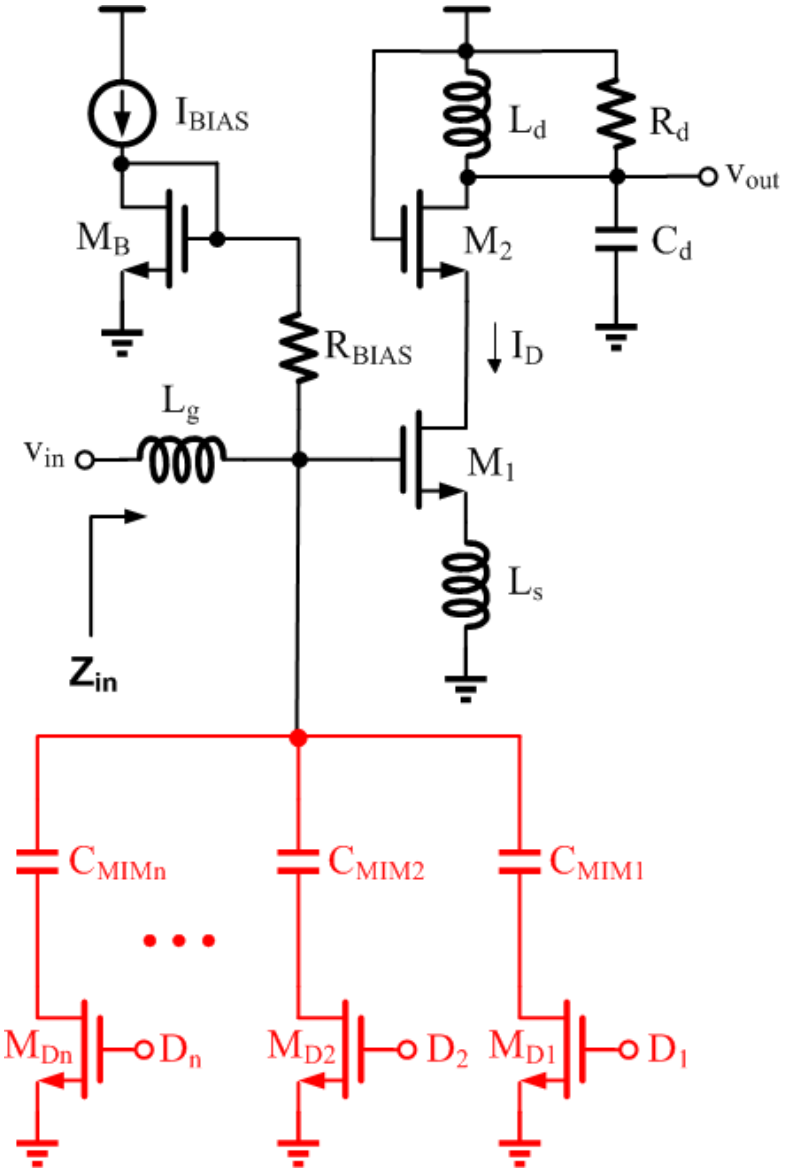
Simulation Results

- Desired matching frequency: 2.4 GHz
- 0.18 μm CMOS technology
- Comparison with transconductance values:



Digitally-Controllable Tuning

- Allows digitally-assisted enhancement of S_{11} to compensate for process variations
- Based on newly proposed equations
- Programmable bank of metal-insulator-metal (MIM) capacitors



Performance with Tuning

	Reference LNA	Tunable LNA
Condition 1: TT models, 27°C, V_{dd}		
S_{11} [dB]	-32.1	-26.4 [00111]
S_{21} [dB]	14.1	14.0
NF [dB]	4.9	5.1
P_{1dB} [dBm]*	-19.0	-17.6
IIP3 [dBm]	-11.4	-9.5
Condition 2: FF models, 85°C, +20% V_{dd}		
S_{11} [dB]	-14.4	-27.0 [01010]
S_{21} [dB]	13.7	13.2
NF [dB]	4.6	5.0
P_{1dB} [dBm]*	-15.2	-13.4
IIP3 [dBm]	-8.7	-6.0
Condition 3: FF models, 85°C, +20% V_{dd}, -15% L_s, -15% L_g		
S_{11} [dB]	-9.4	-19.5 [10000]
S_{21} [dB]	13.8	12.4
NF [dB]	4.5	5.6
P_{1dB} [dBm]*	-15.7	-12.6
IIP3 [dBm]	-8.8	-5.1
Condition 4: SS models, -40°C, -20% V_{dd}		
S_{11} [dB]	-15.6	-32.8 [00011]
S_{21} [dB]	12.6	13.1
NF [dB]	4.5	4.4
P_{1dB} [dBm]*	-20.4	-19.4
IIP3 [dBm]	-12.6	-11.6
Condition 5: SS models, -40°C, -20% V_{dd}, -15% L_s, +15% L_g		
S_{11} [dB]	-8.2	-18.8 [00000]
S_{21} [dB]	12.2	13.4
NF [dB]	4.9	4.4
P_{1dB} [dBm]*	-20.5	-20.4
IIP3 [dBm]	-12.5	-12.4

- Tunable LNA design with almost identical specifications as the reference LNA
- S_{11} improvement: >10dB
- The tuning has small impact on other performance parameters
- Next step:
  Linearity improvement and tuning

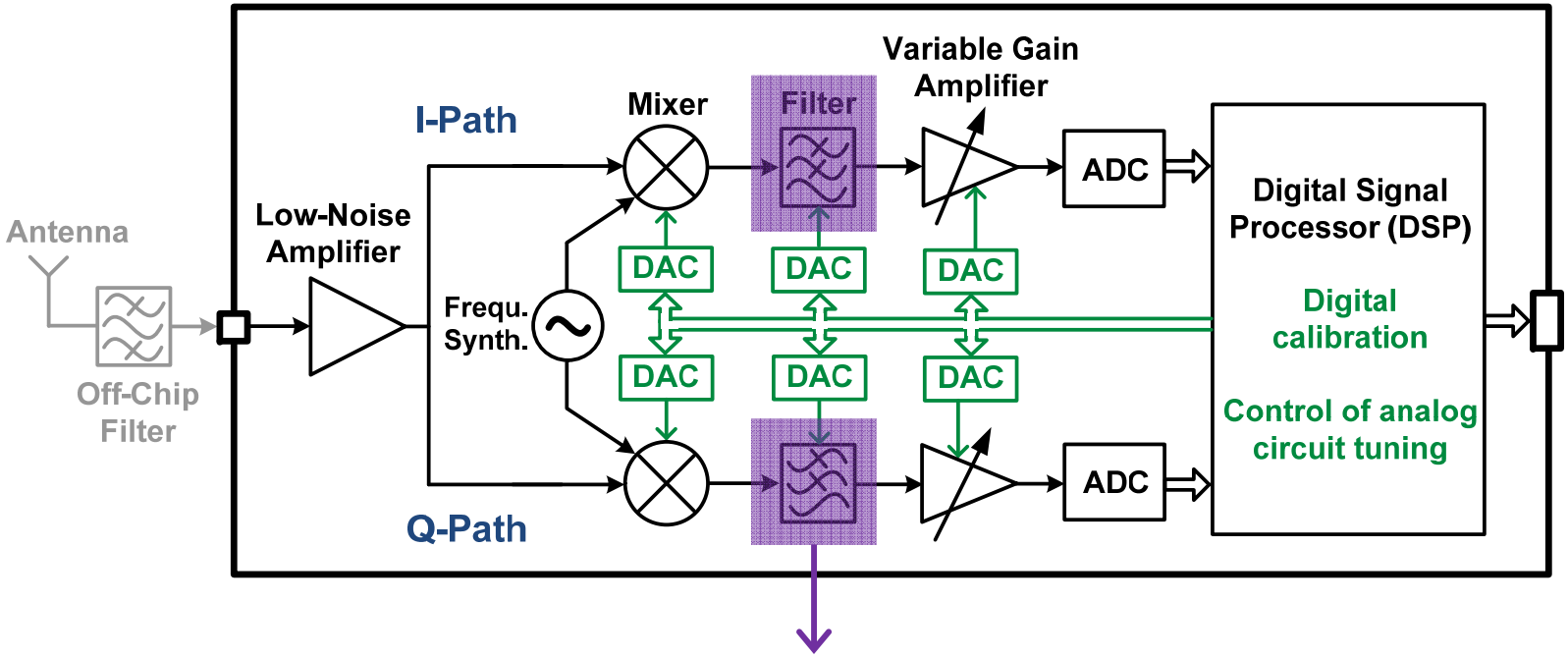
Outline – Lecture 2

- Digitally-assisted analog circuit design & performance tuning
  - LNAs
  - Mixers
  - Filters
  - Example: subthreshold LNA design techniques

- Case study:
  Digitally-assisted linearization of operational transconductance amplifiers

- Case study:
  Variation-aware continuous-time ΔΣ analog-to-digital converter design

Digitally-Assisted Receiver Calibration – Revisited



- Next case study: baseband filter
  - High linearity over wide frequency range
  - Digital programmability

Operational Transconductance Amplifier Linearization

Team at Texas A&M University:

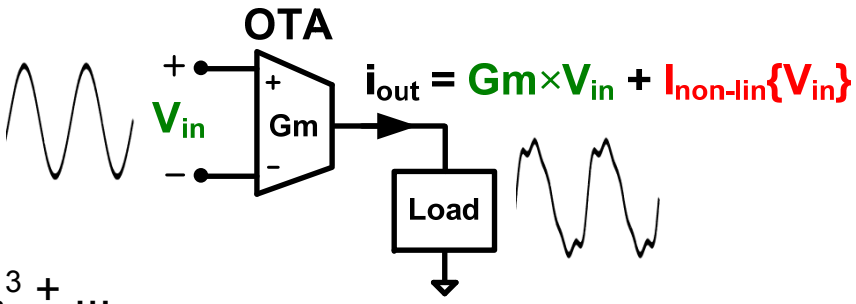
Mohamed Mobarak
Marvin Onabajo
Edgar Sánchez-Sinencio
Jose Silva-Martinez

Motivation for OTA Linearization

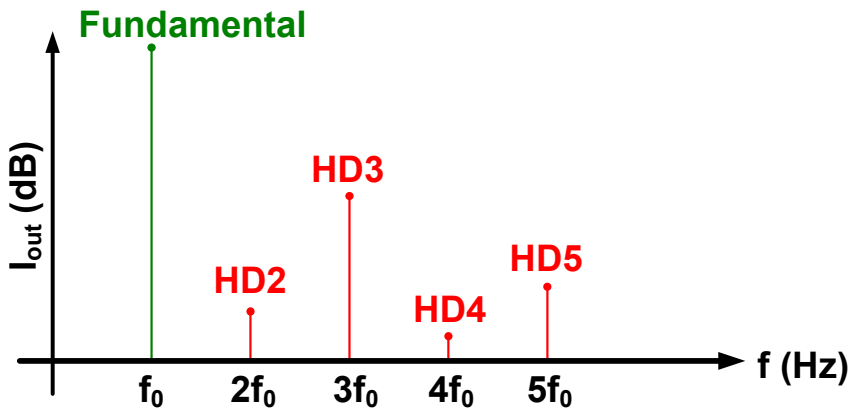
- Applications with operational transconductance amplifiers (OTAs)
  - On-chip filters in the 100-200MHz frequency range
    - In the intermediate frequency stage of wireless receivers
    - Continuous-time ΣΔ analog-to-digital converters
  - Transconductance-capacitor baseband filters
    - Baseband frequency < 50MHz
      (ex. comm. standards: WiMAX, WLAN, WCDMA, UMTS)
    - Third-order intermodulation distortion (IM3) < -60dB
- Project objectives
  - Cancellation of OTA non-linearities (signal distortion reduction)
  - Robustness of the linearization to process variations
  - Compensation for frequency-dependent linearity degradation

The Problem of Limited Linearity

- Mathematical representation of non-linear behavior
  - Amplitude of a sinusoidal input signal: V_{in}
  - Output current (i_{out}) can be expressed as:
    - **Linear:** $i_{lin}\{V_{in}\} = Gm \times V_{in}$
    - **Non-linear:** $i_{non\text{-}lin}\{V_{in}\} = g_{m2} \times V_{in}^2 + g_{m3} \times V_{in}^3 + \ldots$
      where g_{m2}, g_{m3},… are Taylor series coefficients



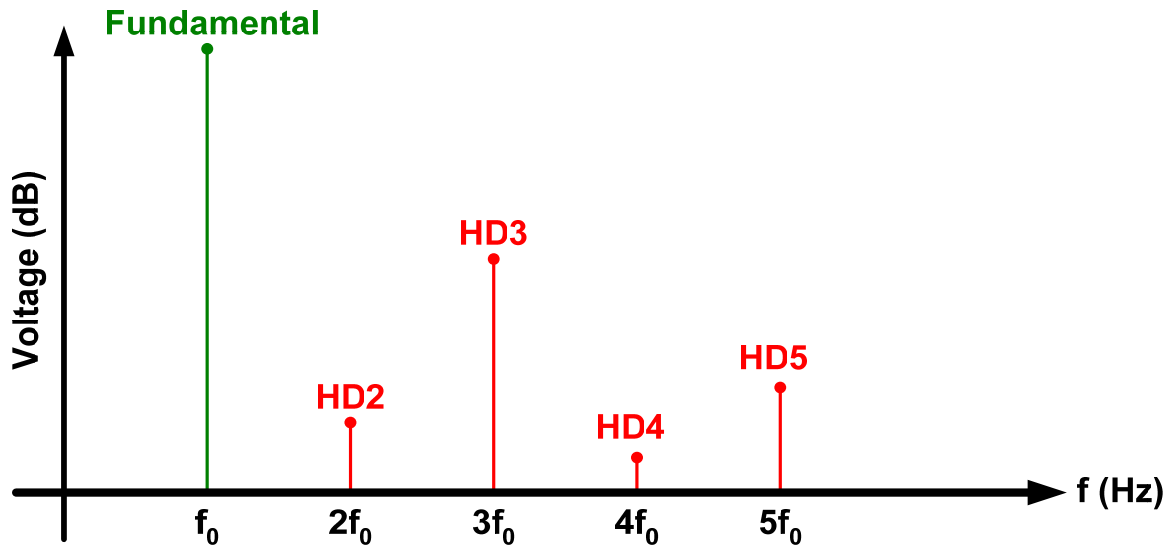
- Practical issues
  - Distorted output current
    - Undesired spectral components at multiples of the frequency f_0 →
    - Typical limit without linearization: HD3 is 50-60dB below the fundamental
  - Frequency dependence: worse linearity at high frequencies



Typical output current spectrum of a fully-differential OTA

Linearization Basics

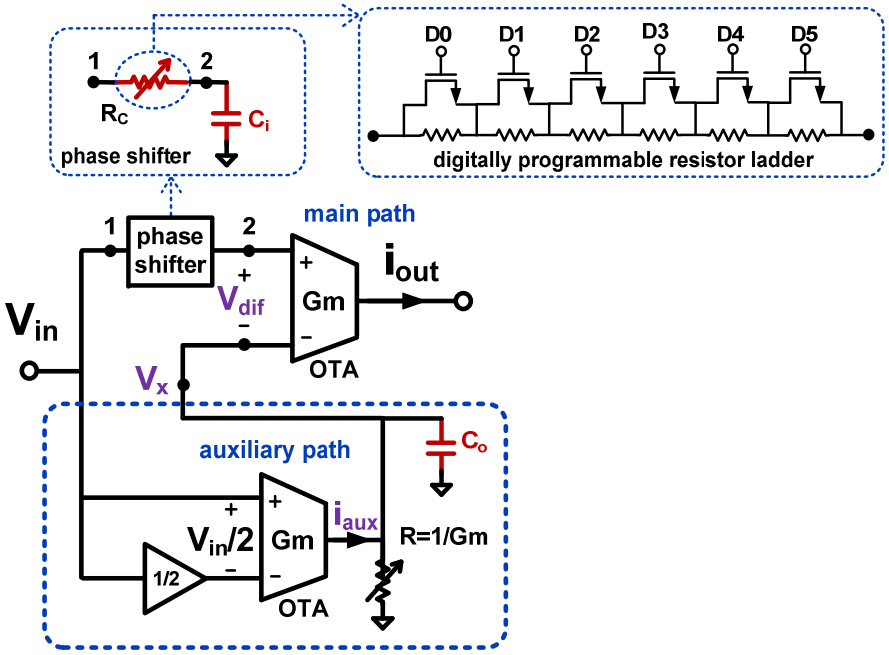
- Linearity Improvement Concepts
  - Harmonics can be reduced by:
    - Signal attenuation
    - Cancellation
    - Feedback
  - Even-order harmonics are suppressed in fully-differential circuits



Spectrum for a fully-differential OTA without odd-order cancellation

Proposed Linearization

- Concept
  - Identical auxiliary path generates the same distortion as in the main path
  - The predistorted signal is subtracted at the input of the OTA in the main path
  - Result: cancellation of distortion
- Effective transconductance
  - Gm_{eff} = ½ Gm of non-linearized OTA with input-attenuation factor of 0.5
  - Same dimensions & operating conditions in both paths
- Conditions for cancellation
  - Gm×R = 1 in aux. path
  - $R_c \approx R$ for optimum cancellation
  - R_c & C_i provide phase shift
    → 1st - order frequency compensation



$i_{aux} = GmV_{in}/2 + i_{non\text{-}lin}\{V_{in}/2\}$

$V_x = V_{in}/2 + i_{non\text{-}lin}\{V_{in}/2\} \times R$

$V_{dif} = V_{in}/2 - i_{non\text{-}lin}\{V_{in}/2\} / Gm$

$i_{out} \approx GmV_{in}/2 + i_{non\text{-}lin}\{V_{in}/2\} - i_{non\text{-}lin}\{V_{in}/2\} \approx GmV_{in}/2$

* $i_{non\text{-}lin}\{V_m\}$ represents the distortion components of the current generated by Gm with input voltage amplitude V_m

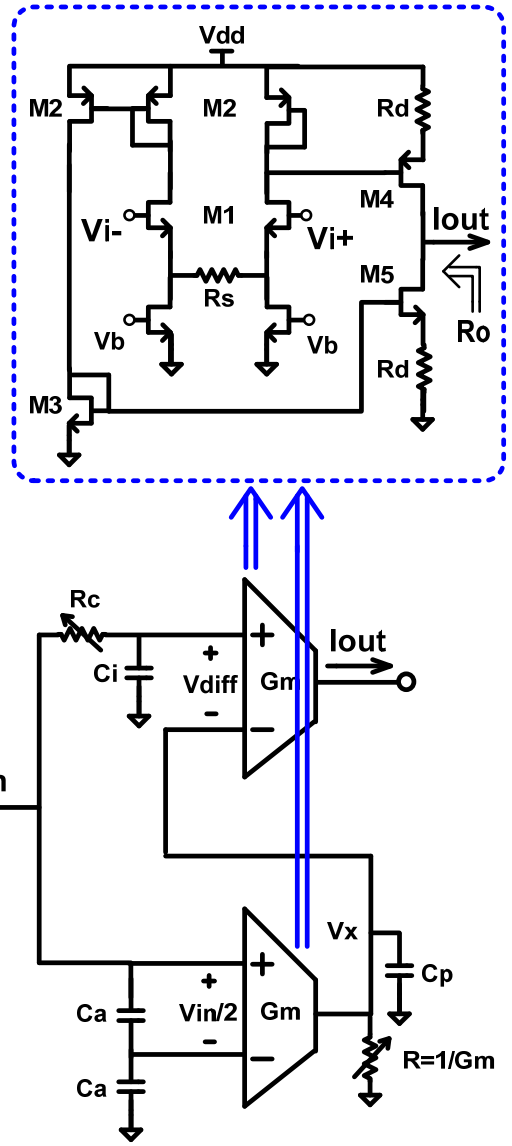
Single-Ended OTA for High-Frequencies

- Topology modified from the typical 3-current mirror OTA
  - Source degeneration resistors (Rd) in the output stage
    - Similar output resistance as a cascode stage with minimum-length transistors in 0.13μm technology
    - High linearity with large signal swings
  - Minimum length transistors (min. parasitic capacitances) for 100MHz operation

- Key component values
  - R = 1.28kΩ ≈ 1/Gm
  - R_c = 1.28kΩ, C_i = 240fF

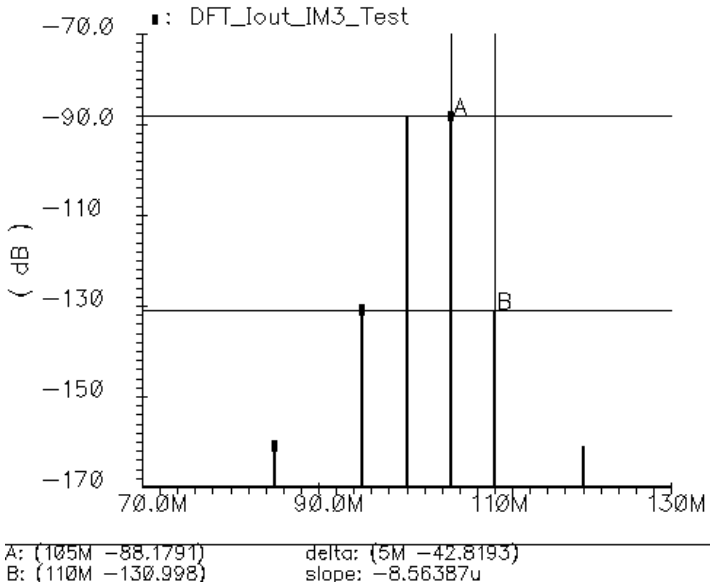
- Basic specifications →
  (0.13μm CMOS, 1.2V supply)

Parameter	Value
Gm	776μA/V
Excess Phase	2.6° at 100MHz
R_o	13kΩ
Gain Bandwidth Product	622MHz
Power	2.4mW

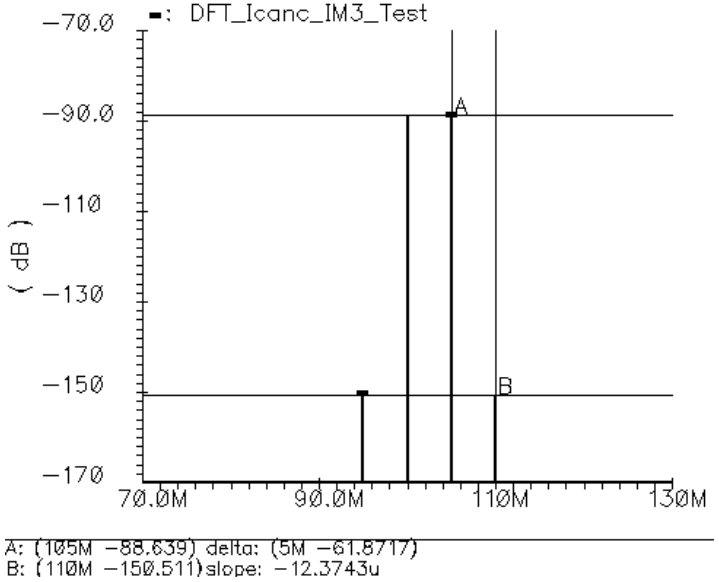


Simulations: Single-Ended OTA

- Output current spectra from IM3 tests
  - $Vin_{peak\text{-}peak}$ = 200mV, test tones at 100MHz and 105MHz
  - Linearity improvements
    - IM3: 19dB, HD2: 28dB, HD3: 30dB
    - THD: 29dB (20dB in a 2nd-order bandpass filter)
  - Trade-offs
    - Noise increase (~1.6x), power consumption (2x), area (2x)

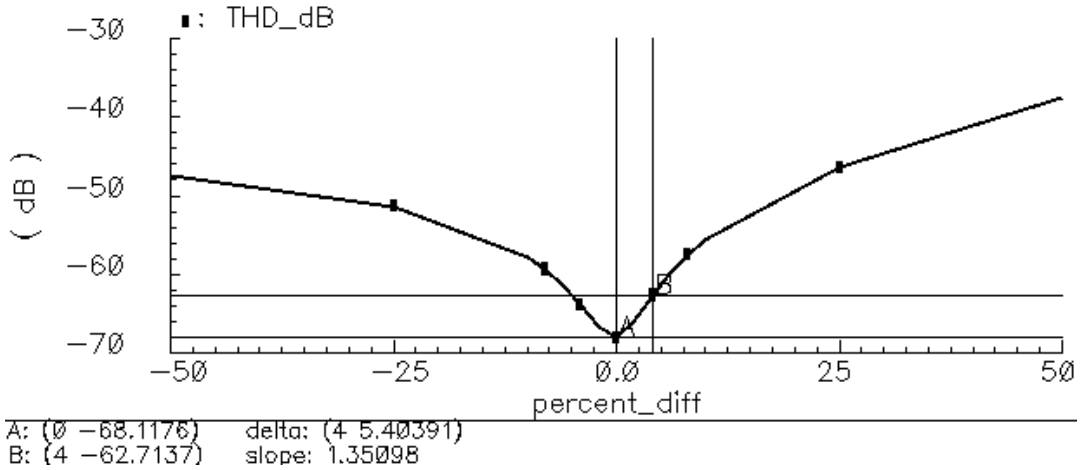


OTA with input-attenuation factor of 0.5
IM3 = -42.8dB at 100MHz



Linearized OTA (attenuation-predistortion)
IM3 = -61.8dB at 100MHz

Variation of Resistor R & Calibration

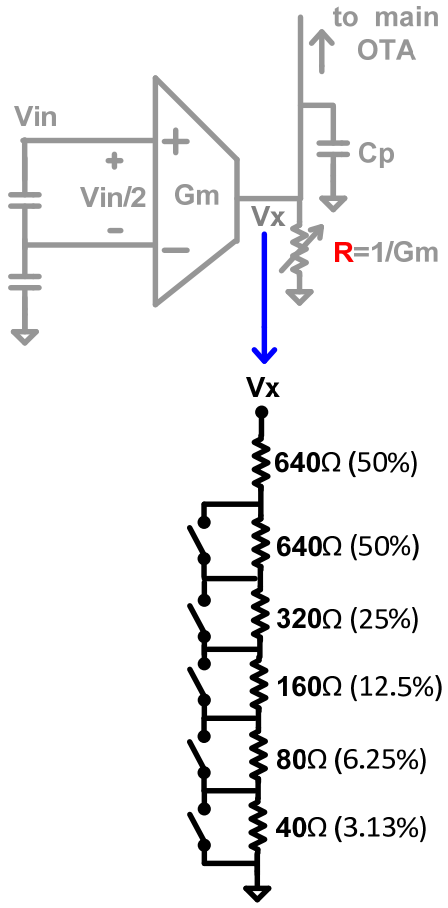


THD vs. %-variation of resistor R

- ΔTHD < 5.4dB requires accuracy of R within 4%

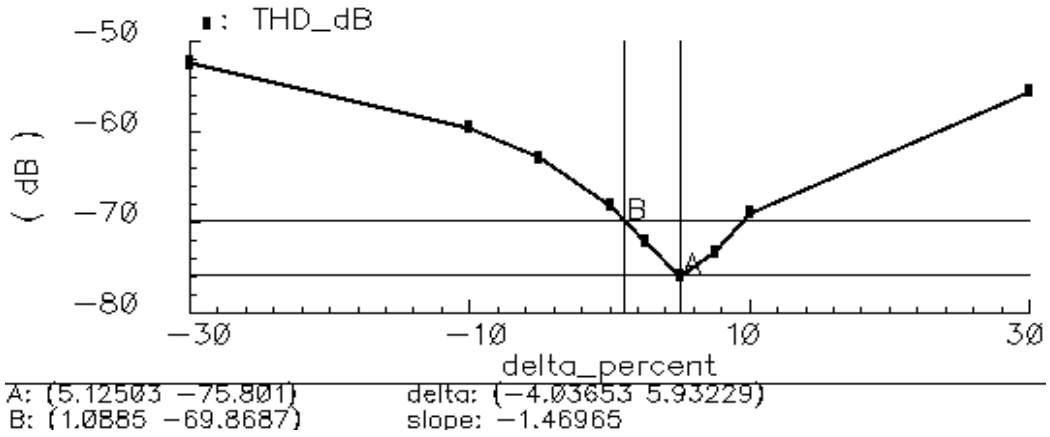
- Some form of calibration is necessary
  - Digital (implemented):
    R can be adjusted with discrete steps until Gm×R = 1
  - Analog tuning also a possibility:
    comparison of Vin and Vx with an error amplifier (Vpeak, Vrms, etc. should be identical), automatic adjustment of R (transistor biased in triode region)

Auxiliary OTA:



Total Rc = 1.28kΩ (this design)

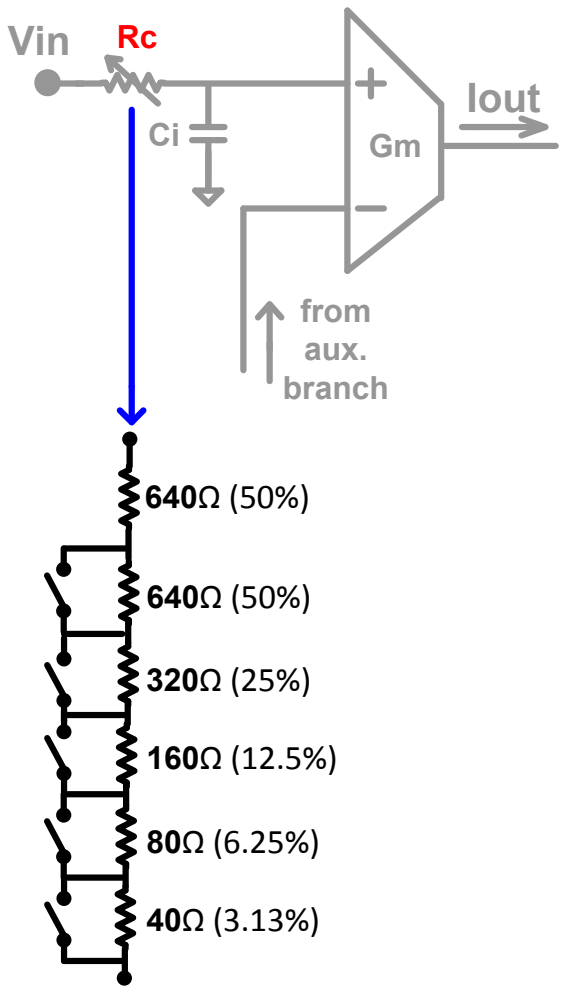
Variation of Resistor Rc & Calibration



THD vs. %-variation of resistor Rc

- ΔTHD < 6dB requires accuracy of Rc within 4%
- Requires same calibration approach as for resistor R
  - Simplest: cycling through switch combinations until optimum linearity
  - Options to assess performance in the digital domain:
    - Monitor HD3 or THD (if A/D, DSP are available)
    - In receivers: monitor bit error rate

Main OTA:



Total Rc = 1.28kΩ (this design)

Single-Ended OTA: Schematic Simulations

Comparison with Vin_{p-p} = 200mV @ 100MHz:

Parameter	Reference OTA	Linearized OTA
$Gm_{effective}$	Gm/2	Gm/2
THD	1.32% (-37.6dB)	0.048% (-66.8dB)
HD2 (below fundamental)	37.68dB	66.68dB
HD3 (below fundamental)	54.35dB	84.26dB
IM3, Δf=5MHz (below fundamental)	42.8dB	61.9dB
Input-referred noise	17.3nV/√Hz	27.7nV/√Hz

Comparison with Vin_{p-p} = 200mV @ 10MHz:

Parameter	Reference OTA	Linearized OTA
$Gm_{effective}$	Gm/2	Gm/2
THD	1.31% (-37.7dB)	0.021% (-73.6dB)
HD2 (below fundamental)	37.78dB	73.49dB
HD3 (below fundamental)	53.88dB	93.03dB
IM3, Δf=0.5MHz (below fundamental)	42.8dB	67.2dB
Input-referred noise	18.7nV/√Hz	29.1nV/√Hz

Fully-Differential OTA Linearization

- Design for high performance
  - High-frequency operation
  - Common-mode noise rejection
  - Differential signal swing (2x larger)
  - Floating-gate transistors as attenuators

- Generalized conditions for attenuation-predistortion linearization
  - Weakly non-linear operation: $k_2 G_m R \le 1$
  - Non-linearity cancellation:

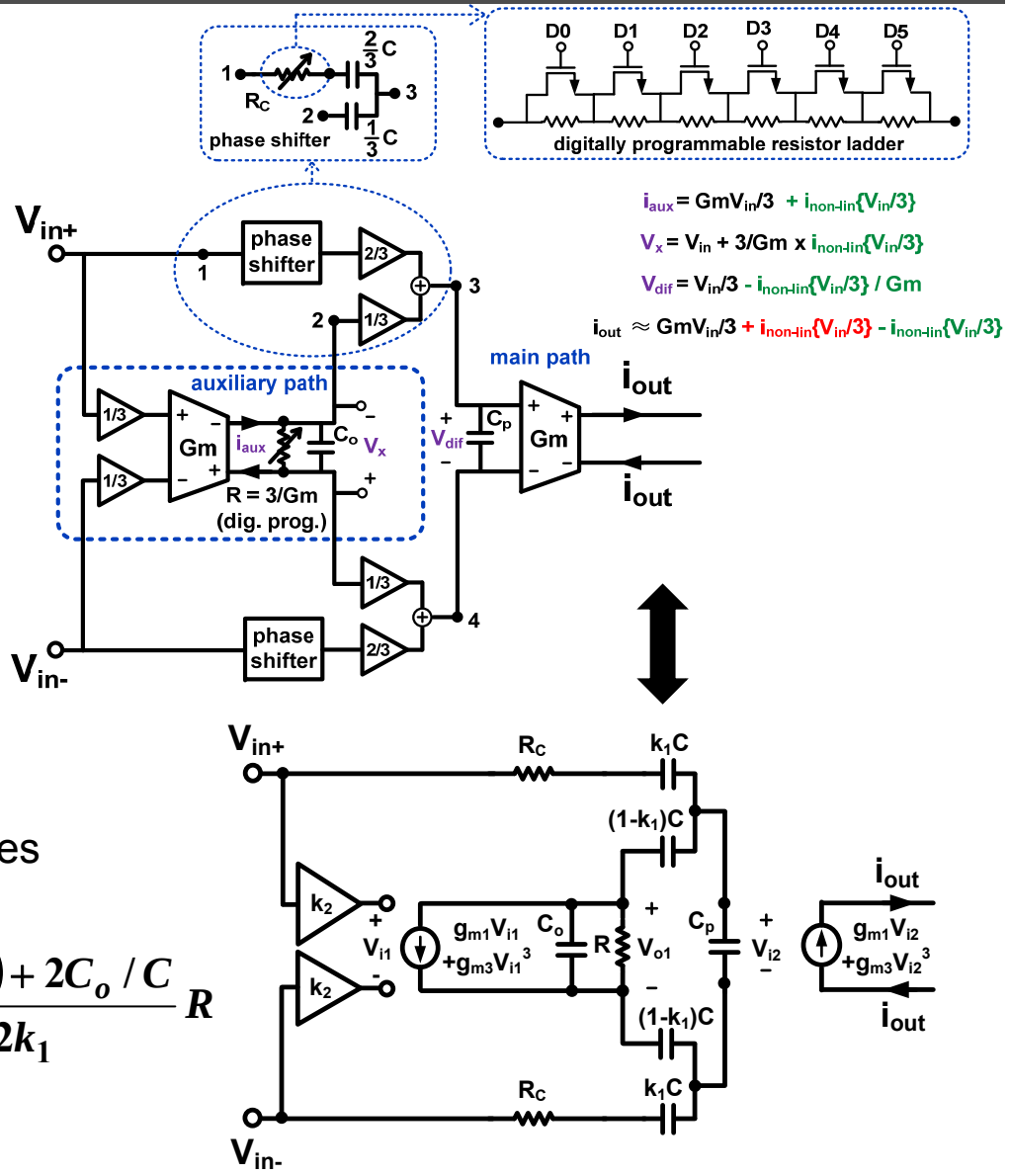
$$(1-k_1)G_m R = 1 \quad , \quad k_2 = k_1/2$$

  - Effective transconductance: $G_{m\_eff} = k_2 G_m$

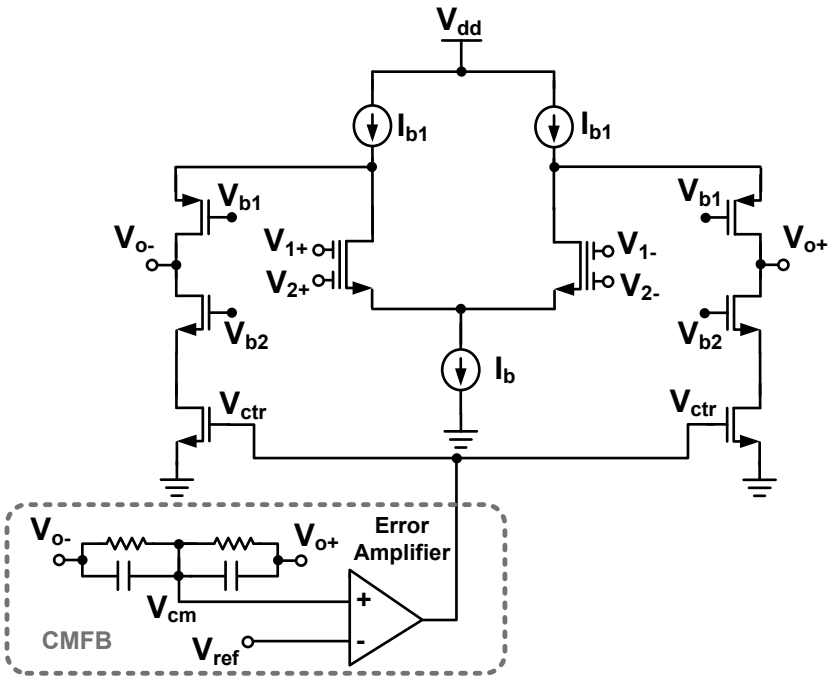
- To ensure IM3 ≈ 0 based on Volterra series analysis to take high-frequency effects of capacitors into account:

$$R_c \approx \frac{(1-k_1)+2C_o/C}{2k_1} R$$

- This design: k_1 = 2/3, k_2 = 1/3
  → R_c=(R/4)*(1+6C_o /C)



Fully-Differential OTA



Folded-cascode OTA

(implements G_m in main and auxiliary paths)

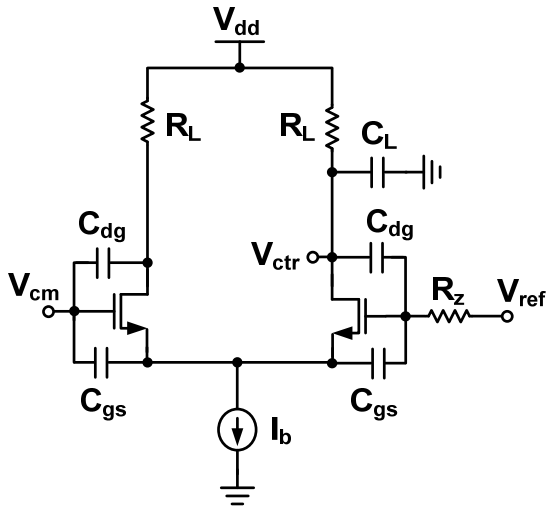
Parameter	Measurement
Transconductance (G_m)	510 µA/V
IM3 @ 50MHz (Vin = 0.2 Vp-p)	-55.3 dB
Noise (input-referred)	13.3 nV/√Hz
Power with CMFB	2.6 mW
PSRR @ 50MHz	48.9 dB
Supply	1.2 V

- Error amplifier compensation with resistor R_z in CMFB extends the bandwidth of the common-mode rejection:

$$GBW \approx \sqrt{A_0 \cdot \omega_{p1} \cdot \omega_{p3}} \approx \sqrt{A_0 \cdot \omega_{p3} \cdot \frac{2}{R_z(C_{gs}/2 + (g_m R_L/2)C_{dg})}}$$

- Affect of R_z on stability according to phase margin (PM):

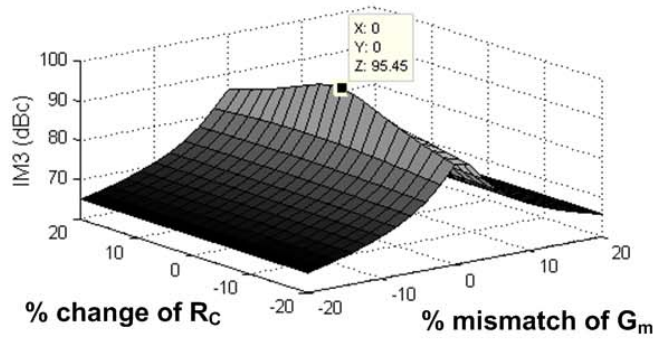
$$PM \approx \tan^{-1}\left(\sqrt{A_0 \cdot \omega_{p3} \cdot \frac{2R_z C_{dg}^2}{(C_{gs}/2 + (g_m R_L/2)C_{dg})}}\right)$$

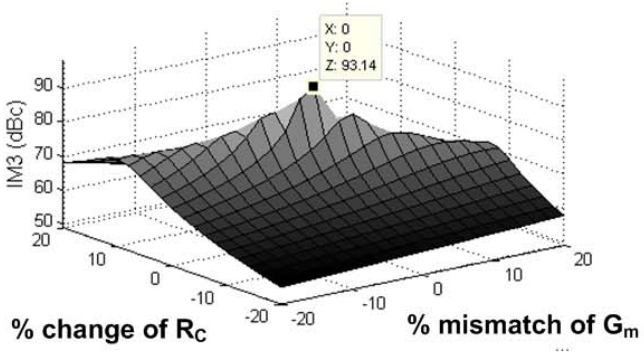


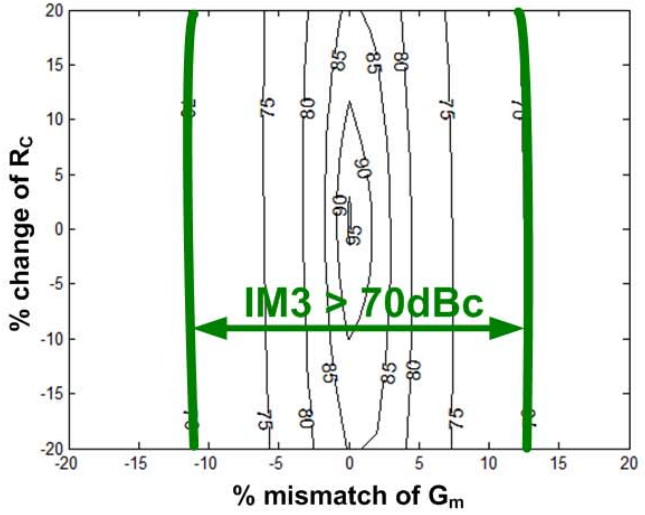
Error amplifier circuit in the common-mode feedback (CMFB) loop

High-Frequency Effects & Process Variation

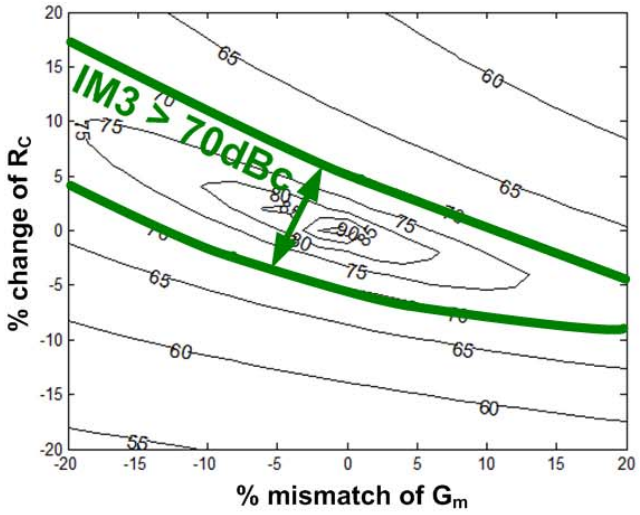
- Theoretical IM3 higher than 70dBc with up to ±10% variation of Gm and ±5% of R_c
  - Not always ensured by matching devices in the layout → programmable resistors for tuning
  - Robustness was verified with schematic corner and component mismatch simulations
- Sensitivity of IM3 (in dBc) to component mismatches:







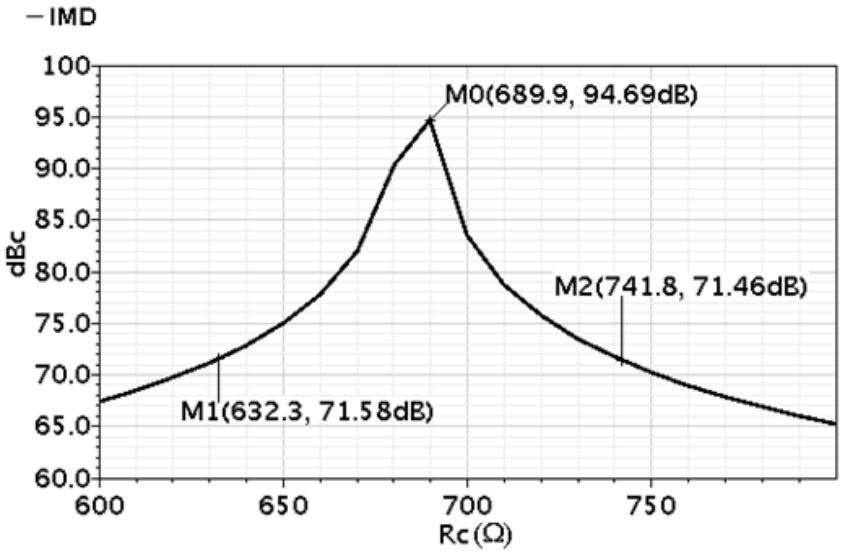
10MHz signal frequency



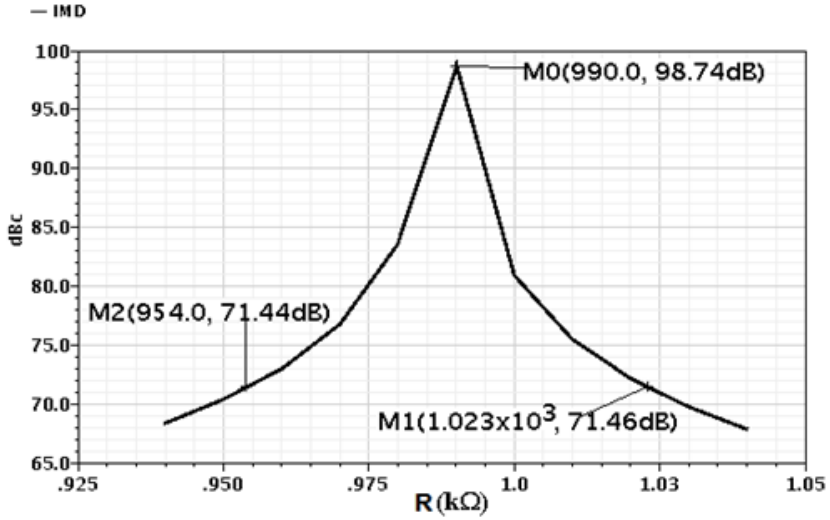
200MHz signal frequency

Simulated Fully-Diff. OTA: Resistor Variations

- IM3 better than 71dBc for ±7.5% Rc-variation
- IM3 better than 71dBc for ±3.3% R-variation in the presence of 10% Gm-mismatch
- Reference OTA has IM3 of 51dBc



IM3 vs. change in R_c at 350MHz



IM3 vs. R with 10% transconductance mismatch between main OTA and auxiliary OTA at 350MHz

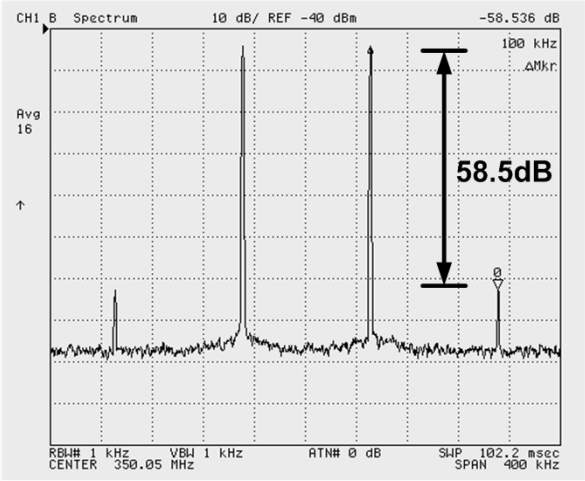
Theoretical IM3:

$$i_{IM3} \approx g_{m3}\left(\frac{k_1/2}{1+2C_p/C}\right)^3\left(3V_{in1}^2V_{in2}/4\right)\left(\frac{1+j\omega_1C\left((1-k_1)R-k_1R_c\right)+2j\omega_1C_oR}{1+j\omega_1b-c\omega_1^2}\right)^2\left(\frac{1-j\omega_1C\left((1-k_1)R-k_1R_c\right)-2j\omega_1C_oR}{1-j\omega_1b-c\omega_1^2}\right)$$

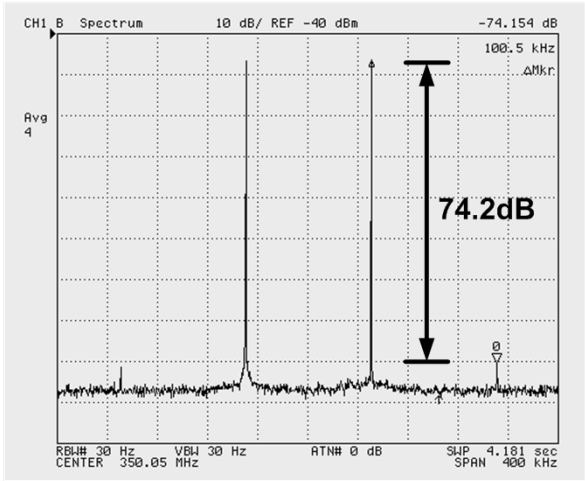
$$-g_{m3}\left(\frac{k_1/2}{1+2C_p/C}\right)^3\left(3V_{in1}^2V_{in2}/4\right)\frac{1+j\omega_1Ck_1R_c}{1+j\omega_1b-c\omega_1^2}$$

Measurements: Standalone OTAs

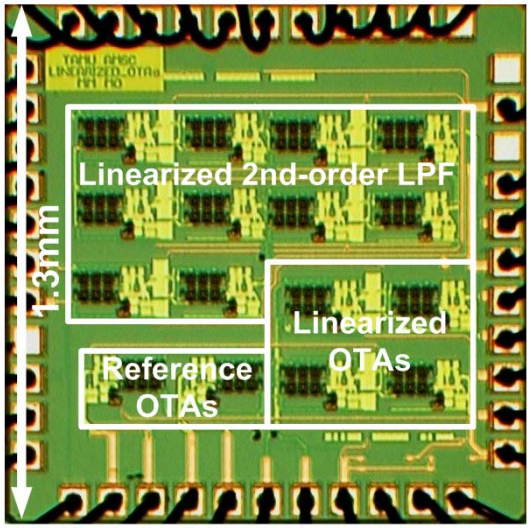
- 0.13μm CMOS Testchip
- Reference OTAs & linearized OTAs (fully-differential → input attenuation = 1/3)



Reference OTA IM3 (input: 0.2V_{p-p}@350MHz)



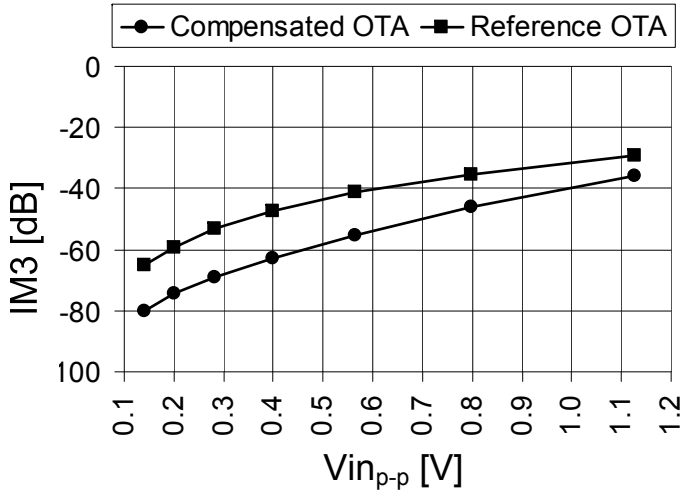
Linearized OTA IM3 (input: 0.2V_{p-p}@350MHz)



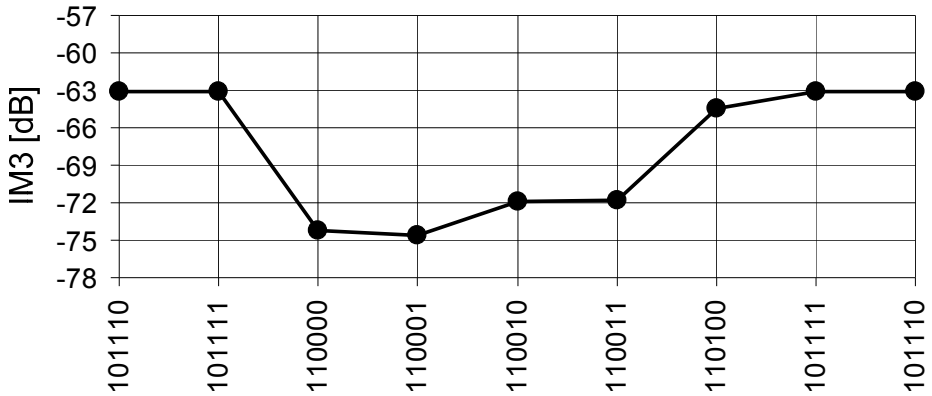
Die micrograph

OTA Type	Input-referred Noise	IM3 (V_{in} = 0.2 V_{p-p})		
		50 MHz	150 MHz	350 MHz
Reference (input attenuation = 1/3)	13.3 nV/√Hz	-55.3 dB	-60.0 dB	-58.5 dB
Linearized (attenuation = 1/3)	21.8 nV/√Hz	-77.3 dB	-77.7 dB	-74.2 dB

Measurements: Standalone OTAs (cont.)



IM3 vs. input voltage for reference OTA and linearized OTA
(two test tones having 100kHz separation around 350MHz)



IM3 dependence of the linearized OTA on phase shift at 350MHz.
(The least significant bit of the digital control code changes the value of phase shift resistor R_c by ~3%)

Fully-Differential OTA Comparison With Previous Works

- Figure of Merit [1]:
  - FOM = NSNR + 10log(f /1MHz) where:
    - NSNR = $SNR_{(dB)}$ + 10log[($IM3_N$ / IM3)(BW / BW_N)(P_N / P_{dis})] from [2]
    - Normalizations:
      SNR integrated over 1MHz, $IM3_N$ = 1%, bandwidth BW_N = 1Hz , power P_N = 1mW
- Competitive performance with respect to the state of the art
  - Effective trade-offs between linearity, power, noise

	[3]* TCAS I 2009	[4]* JSSC 2006	[5] TCAS I 2006	[6] ISSCC 2001	[7]* ISSCC 2005	presented work
IM3	-	-47 dB	-70 dB	-60 dB	-	-74.2 dB
IIP3	-12.5 dBV	-	-	-	7 dBV	7.6 dBV
f	275 MHz	10 MHz	20 MHz	40 MHz	184 MHz	350 MHz
Input voltage	-	0.2 V_{p-p}	1.0 V_{p-p}	0.9 V_{p-p}	-	0.2 V_{p-p}
Power / transconductor	4.5 mW	1.0 mW	4 mW	9.5 mW	1.26 mW	5.2 mW
Input-referred noise	7.8 nV/√Hz	7.5 nV/√Hz	70.0 nV/√Hz	23.0 nV/√Hz	53.7 nV/√Hz	21.8 nV/√Hz
Supply voltage	1.2 V	1.8 V	3.3 V	1.5 V	1.8 V	1.2 V
Technology	65nm CMOS	0.18µm CMOS	0.5µm CMOS	0.18µm CMOS	0.18µm CMOS	0.13µm CMOS
$FOM_{(dB)}$	**87.5**	**92.9**	**96.1**	**99.1**	**100**	**105.6**

* Power/transconductor calculated from filter power. Individual OTA characterization results not reported in full.

OTA Linearization References

- Cited on the previous slide:

[1] A. Lewinski and J. Silva-Martinez, “A high-frequency transconductor using a robust nonlinearity cancellation,” *IEEE Trans. Circuits and Systems II: Express Briefs*, vol. 53, no. 9, pp. 896-900, Sept. 2006.

[2] E. A. M. Klumperink and B. Nauta, “Systematic comparison of HF CMOS transconductors,” *IEEE Trans. Circuits and Systems II: Express Briefs*, vol. 50, no. 10, pp. 728-741, Oct. 2003.

[3] V. Saari, M. Kaltiokallio, S. Lindfors, J. Ryynänen, and K. A. I. Halonen, “A 240-MHz low-pass filter with variable gain in 65-nm CMOS for a UWB radio receiver,” in *IEEE Trans. Circuits and Systems I: Regular Papers*, vol. 56, no. 7, pp. 1488–1499, Jul. 2009.

[4] S. D'Amico, M. Conta, and A. Baschirotto, "A 4.1-mW 10-MHz fourth-order source-follower-based continuous-time filter with 79-dB DR," IEEE J. Solid-State Circuits, vol. 41, no. 12, pp. 2713-2719, Dec. 2006.

[5] J. Chen, E. Sánchez-Sinencio, and J. Silva-Martinez, “Frequency-dependent harmonic-distortion analysis of a linearized cross-coupled CMOS OTA and its application to OTA-C filters,” *IEEE Trans. Circuits and Systems I: Regular Papers*, vol. 53, no. 3, pp. 499-510, March 2006.

[6] D. Yongwang and R. Harjani, "A +18 dBm IIP3 LNA in 0.35μm CMOS," in *ISSCC Dig. Tech. Papers*, pp.162-163, Feb. 2001.

[7] J. C. Rudell, O. E. Erdogan, D. G. Yee, R. Brockenbrough, C. S. G. Conroy, and B. Kim, "A 5th-order continuous-time harmonic-rejection GmC filter with in-situ calibration for use in transmitter applications," in *ISSCC Dig. Tech. Papers*, pp. 322-323, Feb. 2005.

OTA Linearization without Increased Power

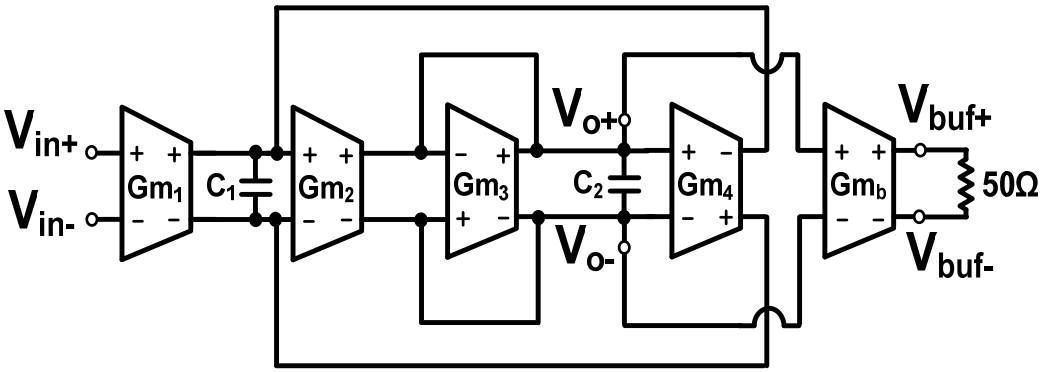
- Requires redesign of the OTA with 50% of the initial bias current
  - Increased W/L ratio to maintain the same transconductance value
  - Parasitic capacitances of the larger devices lead to bandwidh (f_{3dB}) reduction
  - Gate-source overdrive (saturation) voltage is approximately 50% less

- Trade-off to maintain similar transconductance and +20dB linearity enhancement without power increase: Bandwidth reduction

- Example – Comparison after linearization (redesign of the fully-differential OTA) with the same power consumption as the non-linearized reference OTA:

OTA type	V_{DSAT} of input diff. pair	f_{3db} with 50Ω load	Input-referred noise	Power	IM3 (V_{in} = 0.2 V_{p-p})	Normalized |FOM| (at f_{max})
Reference (input attenuation = 1/3)	90 mV	2.49 GHz	9.7 nV/√Hz	2.6 mW	-53.1 dB at f_{max} = 350MHz (-53.2 dB at 100MHz)	57.2
Linearized (attenuation = 1/3 & compensation)	54 mV	1.09 GHz	14.3 nV/√Hz	2.6 mW	-77.1 dB at f_{max} = 100MHz	119.2

Measurements: Filter with Linearized OTAs



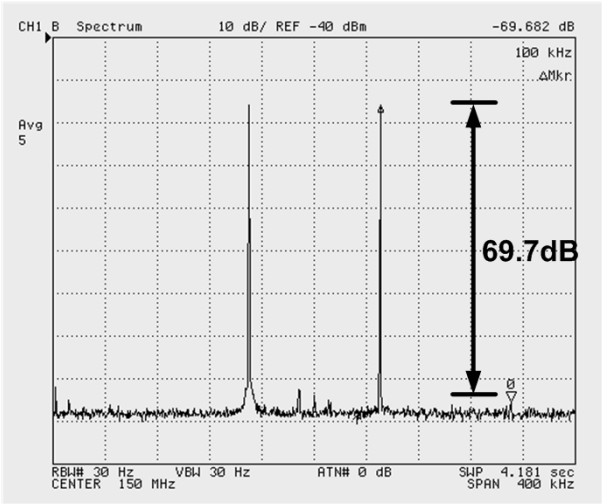
2nd-order low-pass filter diagram

Parameter	Value
Corner frequency (f_{3db})	194.7 MHz
Passband gain	0 dB
Quality factor	1
$Gm_{1,2,3,4}$	510 µA/V

- IM3 ≈ -70dB up to 150MHz (with 0.2V_{p-p} input)
- Broadband linearity thanks to the phase shifter

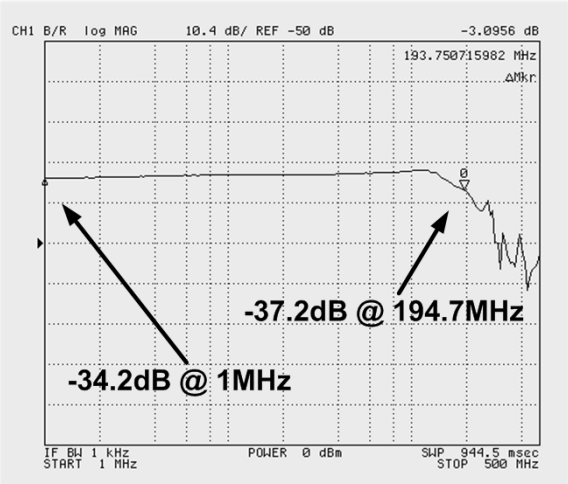
  (IM3 = -66.1dB at 200MHz, filter corner frequ. = 194.7MHz)

Linearized Filter	IM3 (V_{in} = 0.2 V_{p-p})			
	50 MHz	100 MHz	150 MHz	200 MHz
	-73.9 dB	-69.6 dB	-69.7 dB	-66.1 dB

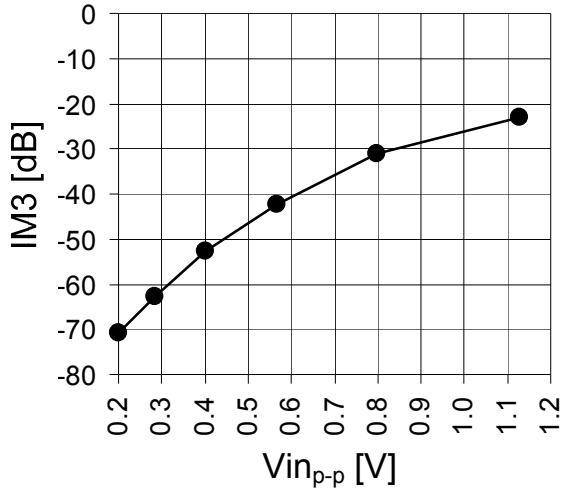


IM3 with compensated OTAs (input: 0.2V_{p-p}@150MHz)

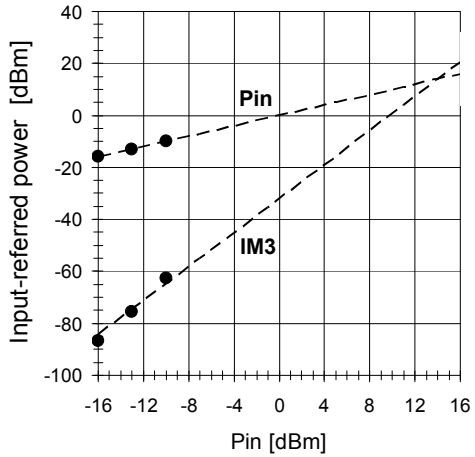
Measurements: Filter with Fully-Differential OTAs



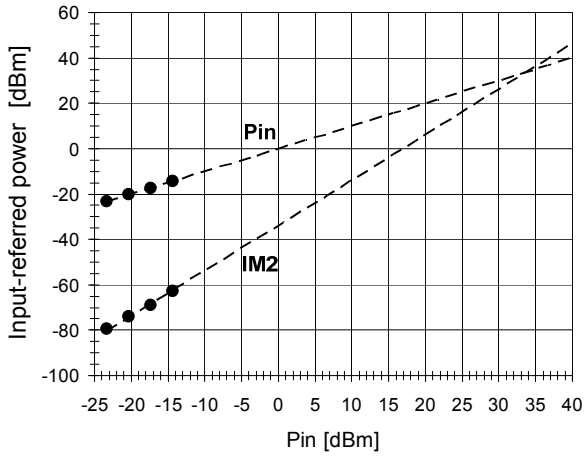
Frequency response of the 2nd - order low-pass filter



IM3 vs. input peak-peak voltage (two test tones having 100kHz separation around 150MHz)



IIP3 = 14.0dBm
(two tones, Δf = 100kHz around 150MHz)



IIP2 = 13.4dBm
(two tones, Δf = 100kHz around 2MHz)

Wideband G_m-C Low-Pass Filter Comparison

	[A]	[B]	[C]	[D]	[E]	[F]	[G]	presented work
Filter order	5	5	8	4	7	5	3	2
f_c (max.)	275MHz	184MHz	120MHz	200MHz	200MHz	500MHz	300MHz	200MHz
Signal swing	-	$0.30V_{p-p}$	$0.20V_{p-p}$	$0.88V_{p-p}$	$0.80V_{p-p}$	$0.50V_{p-p}$	-	$0.75V_{p-p}$
Linearity with max. Vin_{p-p}	-	HD3, HD5: < -45dB	THD: -50dB @ 120MHz	THD: -40dB @ 20MHz	THD: -42dB @ 200MHz	THD: < -40dB @ 70MHz	-	THD < -40dB @ 150MHz
In-band IIP3	-12.5dBV (0.5dBm)	7dBV (20dBm)	-	-	-	-	3.9dBV (16.9dBm)	1.0dBV (14.0dBm)
In-band IIP2	-	-	-	-	-	-	19dBV (32dBm)	20.7dBV (33.7dBm)
Out-of-band IIP3	-8dBV (5dBm)	-	-	-	-	-	-	-0.6dBV (12.4dBm)
Out-of-band IIP2	15dBV (28dBm)	-	-	-	-	-	-	17.4dBV (30.4dBm)
Power	36mW	12.6mW	120mW	48mW	210mW	100mW	72mW	20.8mW
Power per pole	7.2mW	2.5mW	15mW	12mW	30mW	20mW	24mW	10.4mW
Input-referred noise	7.8nV/√Hz	53.7nV/√Hz	-	-	-	-	5nV/√Hz	35.4nV/√Hz
Dynamic range	44dB	43.3dB	45dB	58dB	-	52dB	-	54.5dB
Supply voltage	1.2V	1.8V	2.5V	2V	3V	3.3V	1.8V	1.2V
Technology	65nm CMOS	180nm CMOS	250nm CMOS	350nm CMOS	250nm CMOS	350nm CMOS	180nm CMOS	130nm CMOS

[A] V. Saari, M. Kaltiokallio, S. Lindfors, J. Ryynänen, and K. A. I. Halonen, "A 240-MHz low-pass filter with variable gain in 65-nm CMOS for a UWB radio receiver," *IEEE Trans. Circuits and Systems I: Regular Papers*, vol. 56, no. 7, pp. 1488-1499, July 2009.

[B] E. Sánchez-Sinencio and J. Silva-Martinez, "CMOS transconductance amplifiers, architectures and active filters: a tutorial," *IEE Proc. Circuits, Devices and Systems*, vol. 147, pp. 3-12, Feb. 2000.

[C] G. Bollati, S. Marchese, M. Demicheli, and R. Castello, "An eighth-order CMOS low-pass filter with 30-120 MHz tuning range and programmable boost," *IEEE J. Solid-State Circuits*, vol. 36, no. 7, pp. 1056-1066, July 2001.

[D] A. Otin, S. Celma, and C. Aldea, "A 40–200 MHz programmable 4th-order Gm-C filter with auto-tuning system," in *Proc. 33rd Eur. Solid-State Circuits Conf. (ESSCIRC)*, pp. 214-217, Sept. 2007.

[E] S. Dosho, T. Morie, and H. Fujiyama, "A 200-MHz seventh-order equiripple continuous-time filter by design of nonlinearity suppression in 0.25-μm CMOS process," *IEEE J. Solid-State Circuits*, vol. 37, no. 5, pp. 559-565, May 2002.

[F] S. Pavan and T. Laxminidhi, "A 70-500MHz programmable CMOS filter compensated for MOS nonquasistatic effects," in *Proc. 32nd Eur. Solid-State Circuits Conf. (ESSCIRC)*, pp. 328-331, Sept. 2006.

[G] K. Kwon, H.-T. Kim, and K. Lee, "A 50–300-MHz highly linear and low-noise CMOS Gm-C filter adopting multiple gated transistors for digital TV tuner ICs," *IEEE Trans. Microwave Theory and Techniques*, vol. 57, no. 2, pp. 306-313, Feb. 2009.

OTA Linearization: Summary & Conclusions

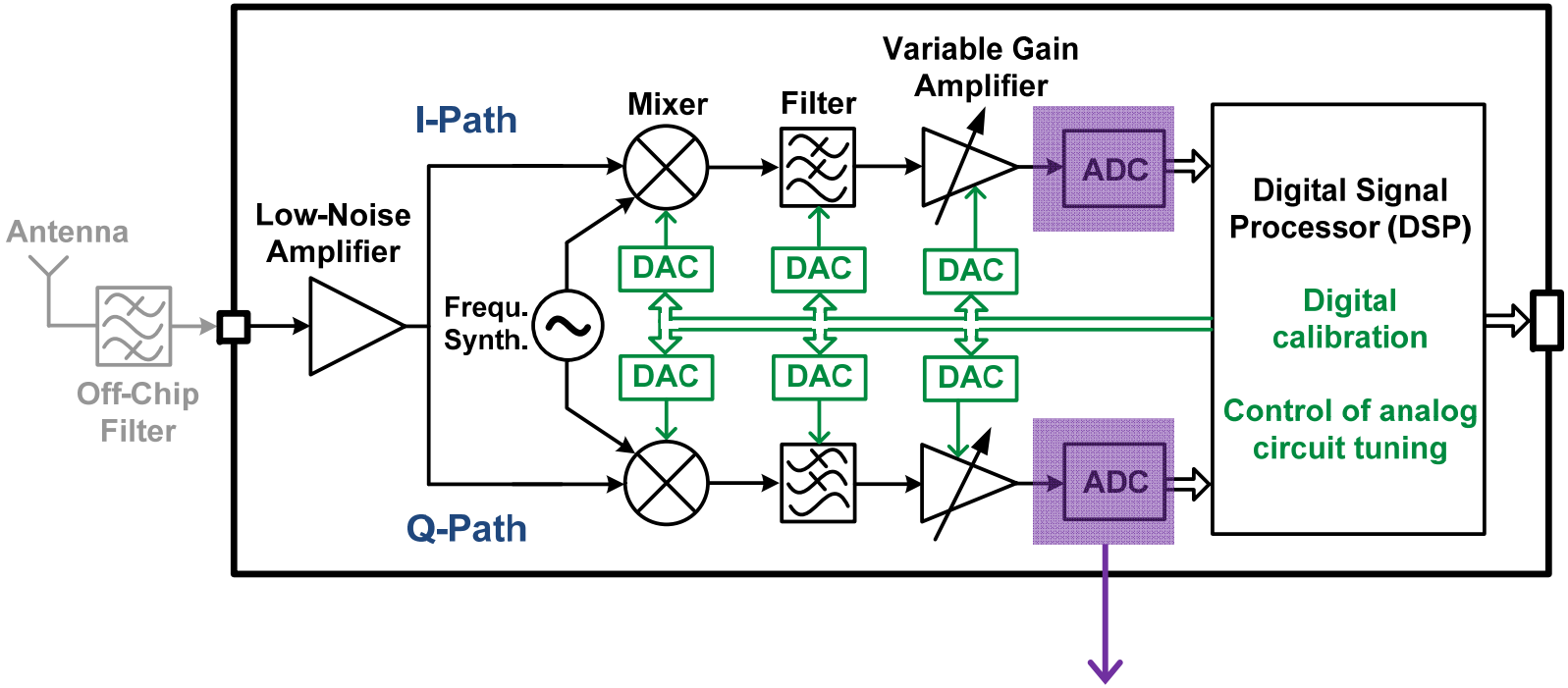
- Proposed linearization technique
  - For OTAs in transconductance-C filter applications
  - Independent of the OTA circuit topology
  - Allows linearity, noise, power design trade-offs
- Measured performance
  - IM3 improvement of up to 22dB
  - Performance meets state-of-the-art requirements
- Compensation for PVT variations and high-frequency effects
  - Based on digital adjustment of resistors
  - Main amplifier can be optimized for its target application (no internal circuit design change due to the linearization scheme)

M. Mobarak, M. Onabajo, J. Silva-Martinez, and E. Sánchez-Sinencio, "Attenuation-predistortion linearization of CMOS OTAs with digital correction of process variations in OTA-C filter applications," *IEEE J. Solid-State Circuits*, vol. 45, no. 2, pp. 351-367, Feb. 2010.

Outline – Lecture 2

- Digitally-assisted analog circuit design & performance tuning
  - LNAs
  - Mixers
  - Filters
  - Example: subthreshold LNA design techniques
- Case study: Digitally-assisted linearization of operational transconductance amplifiers
- Case study: Variation-aware continuous-time ΔΣ analog-to-digital converter design

Digitally-Assisted Receiver Calibration – Revisited



- Next case study: continuous-time ΔΣ analog-to-digital converter design
  - High Signal-to-noise-and-distortion ratio (SNDR) over wide bandwidth
  - Robustness to performance degradation from component mismatches

Variation-Aware Continuous-Time ΔΣ Analog-to-Digital Converter Design

Team at Texas A&M University:

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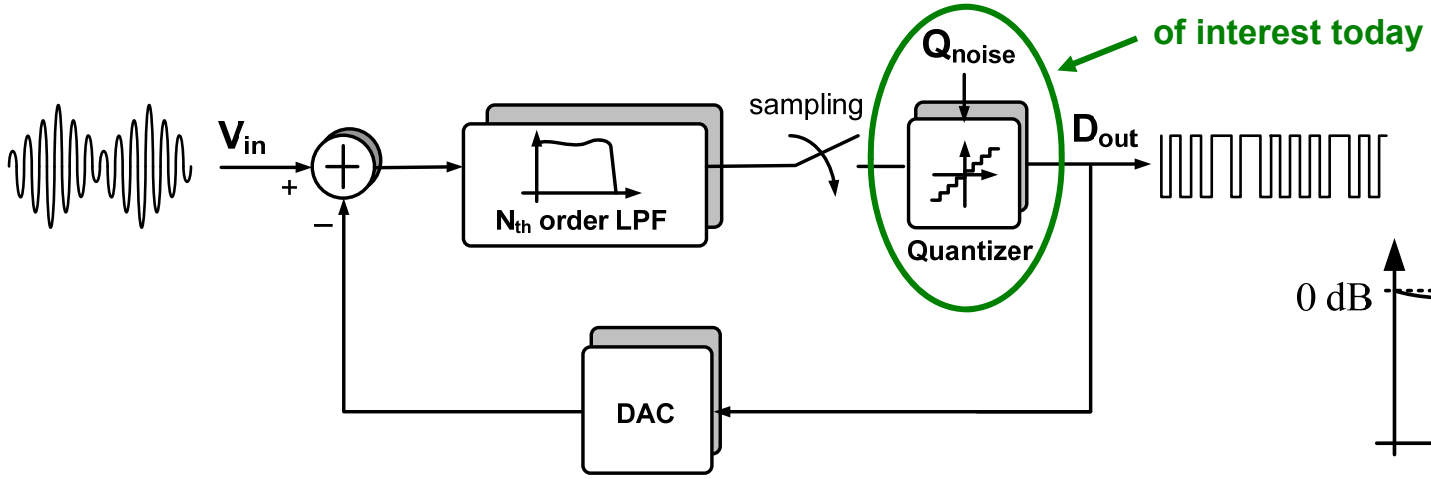
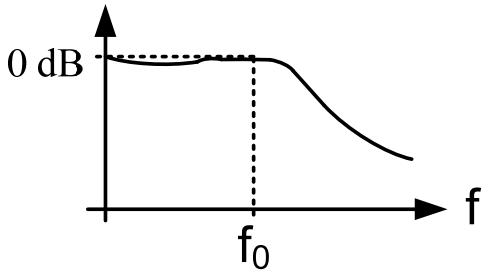
Venkata Gadde, Yung-Chung Lo,
Hsien-Pu Chen, Vijay Periasamy,
Jose Silva-Martinez

Specific Quantizer Application Overview

- Analog-to-digital converter (ADC) group project
  - Continuous-time low-pass ΣΔ modulator with competitive specifications
    - 25MHz bandwidth, sampling frequency = 400MHz
    - Signal-to-noise-and-distortion ratio (SNDR) = 67.7dB
    - Power consumption = 48mW
  - Robustness to performance degradation from component mismatches
    - Device mismatches → non-linearities (signal distortion) → SNDR degradation
    - Novel multi-bit feedback with a single-element digital-analog-converter (DAC) using pulse width modulation (PWM)
      → Avoids non-linearities from unit element mismatches (encountered in conventional multi-bit DACs)
- Presentation focus: 3-bit quantizer
  - Proposed topology is optimized for the PWM DAC approach (multiple clock phases)
  - Option for adjusting quantization levels to compensate for process variations

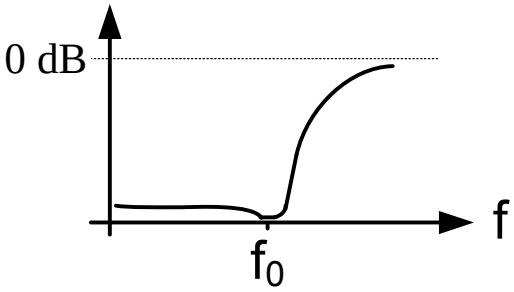
Basic ΣΔ Modulation Concepts





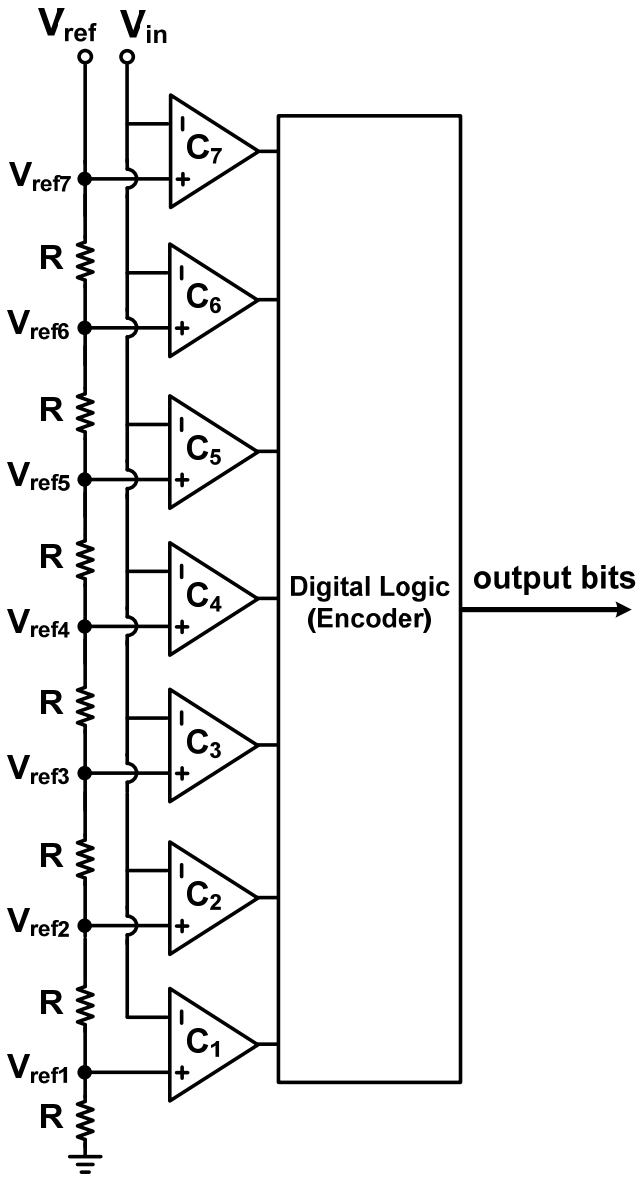
$$STF = \frac{D_{out}}{V_{in}} \frac{A}{1+A}$$

- Highlights of relevant multi-bit DAC/quantizer effects:
  - Reduced quantization noise → $\sigma_{(quant.\,noise)} = \frac{V_{full\text{-}swing}}{2^{bits} \cdot \sqrt{12}}$
  - Improved stability
  - DAC non-linearity at V_{in} is not suppressed by the feedback loop!
    → More sensitivity to mismatches from process variations!

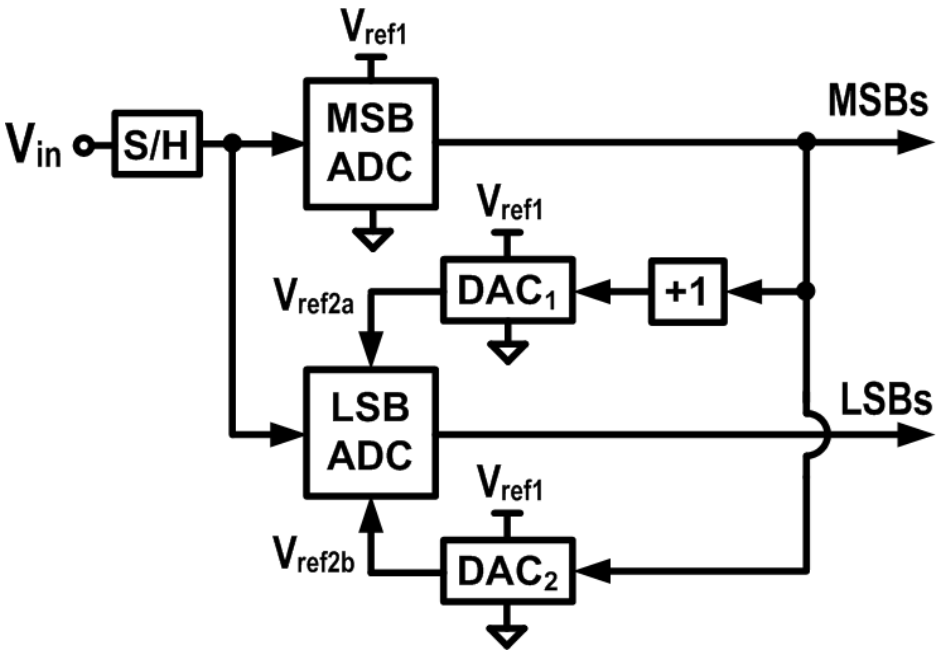


$$NTF = \frac{D_{out}}{Q_{noise}} = \frac{1}{1+A}$$

Conventional 3-Bit Flash Quantizer



Two-Step ADC Principle



- Subranging
  - Most-significant bit(s) (MSB) are resolved first (fixed reference V_{ref1})
  - Least-significant bit(s) (LSB) are quantized with variable references V_{ref2a} and V_{ref2b}

    $\rightarrow V_{ref2a}$ and V_{ref2b} depend on the MSB value
- Multi-step quantization can reduce area and power consumption when a delay of multiple clock cycles is acceptable

J. Doernberg, P. R. Gray, and D. A. Hodges, "A 10-bit 5-Msample/s CMOS two-step flash ADC," *IEEE J. Solid-State Circuits*, vol. 24, no. 2, pp. 241-249, April 1989.

Modern “Flash-like” ADC Examples

- Alternative architectures take advantage of technology scaling (fast switching)
  - Enhanced performance at higher conversion speeds
  - Reduced power consumption
  - Improving compatibility with digital CMOS processes

- Folding flash ADC
  - Comprised of 16 instead of 31 (conventional flash) comparators for 5-bit resolution
  - 1.75 GS/s in 90nm CMOS, 2.2mW, 5-bit res.

  B. Verbruggen, J. Craninckx, M. Kuijk, P. Wambacq, and G. Van der Plas, "A 2.2 mW 1.75 GS/s 5 bit folding flash ADC in 90 nm digital CMOS," *IEEE J. Solid-State Circuits*, vol. 44, no. 3, pp.874-882, March 2009.

- Asynchronous ADC
  - Asynchronous successive approximations performed with a single comparator
  - Input is weighted against a reference that is changed with a switchable capacitor array
  - 600-MS/s in 0.13µm CMOS, 5.3-mW

  S.-W. Chen and R. W. Brodersen, "A 6-bit 600-MS/s 5.3-mW asynchronous ADC in 0.13-µm CMOS," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2669-2680, Dec. 2006.

More Modern “Flash-like” ADC Examples

- Two-step ADC
  - MSB is quantized first
  - LSBs are determined with an asynchronous binary-search procedure
  - 150MS/s in 90nm CMOS, 133μW, 7-bit res.

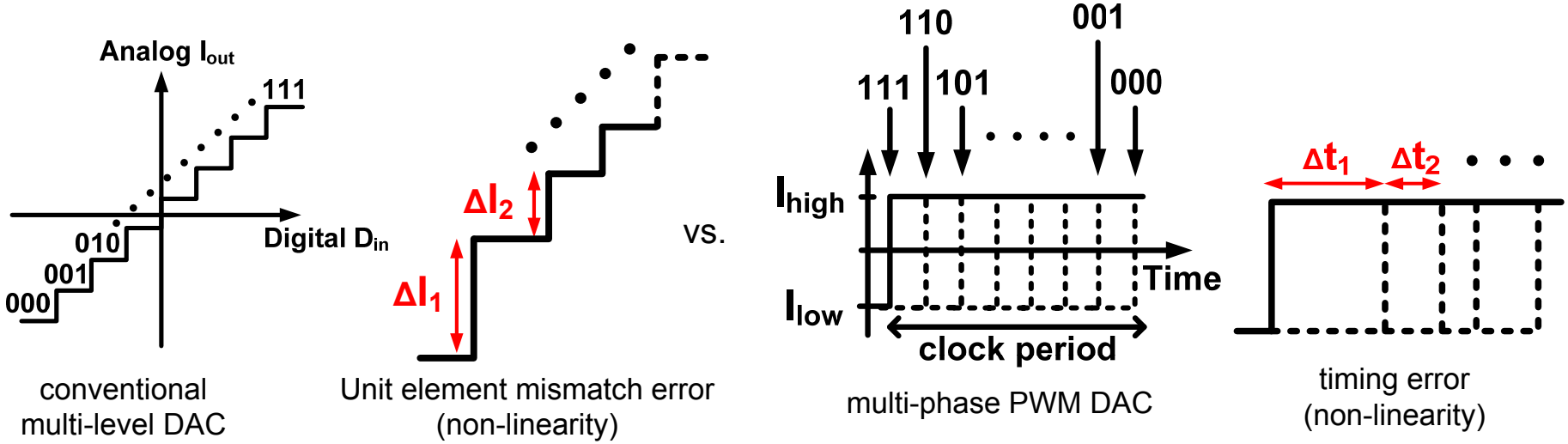
  G. Van der Plas and B. Verbruggen, "A 150MS/s 133μW 7b ADC in 90nm digital CMOS using a comparator-based asynchronous binary-search sub-ADC," in *IEEE Intl. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2008, pp. 242-243, 610.

- Other related references:

  J. Craninckx and G. Van der Plas, "A 65fJ/conversion-step 0-to-50MS/s 0-to-0.7mW 9b charge-sharing SAR ADC in 90nm digital CMOS," in *IEEE Intl. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2007, pp. 246-247, 600.

  L. Dorrer, F. Kuttner, P. Greco, P. Torta, and T. Hartig, "A 3-mW 74-dB SNR 2-MHz continuous-time delta-sigma ADC with a tracking ADC quantizer in 0.13-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2416- 2427, Dec. 2005.

Taking Advantage of Fast-Switching



conventional multi-level DAC

Unit element mismatch error (non-linearity)

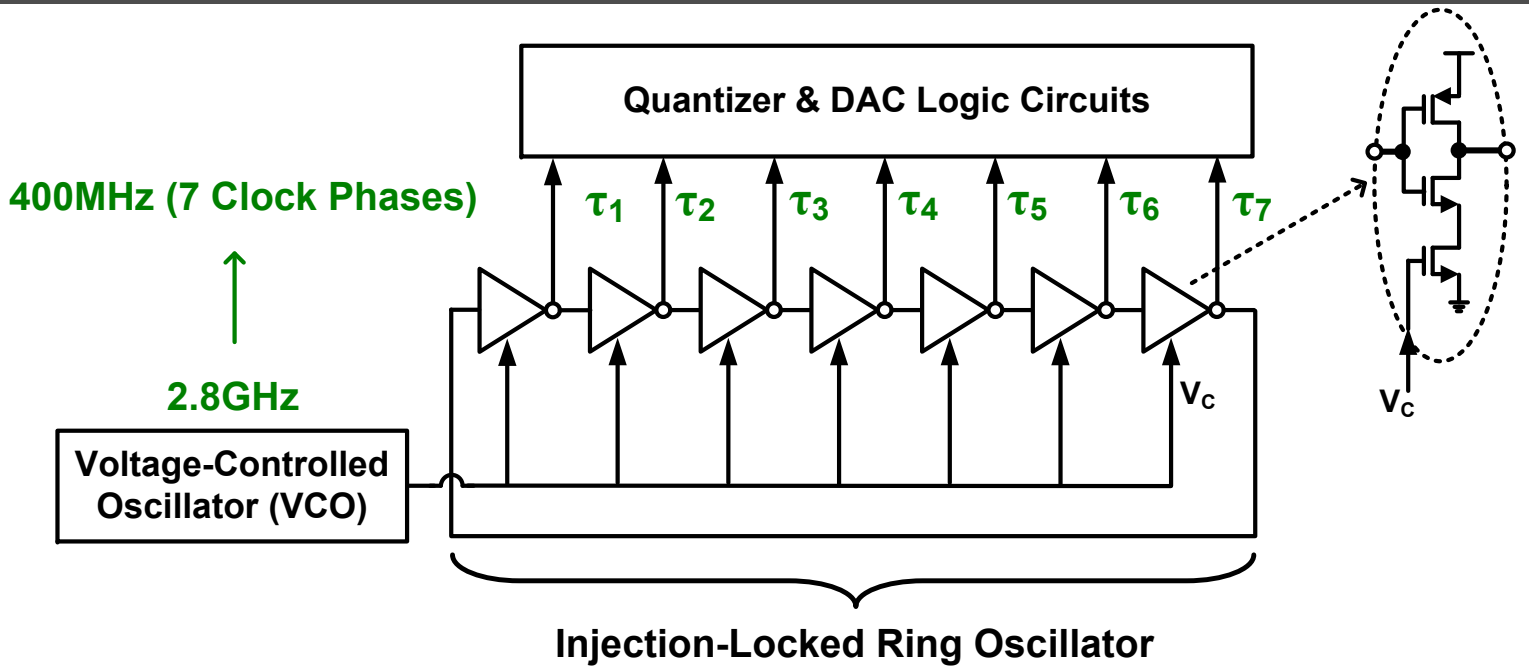
multi-phase PWM DAC

timing error (non-linearity)

- Multi-phase digital-analog-converter (DAC) & quantizer approach
  - Exploits the inherent linearity of the single-element DAC
  - Same charge injected into the filter as with the conventional multi-bit feedback DAC
  - Multi-bit feedback with a single-element DAC
    - No element mismatch, low layout complexity, low power
    - 7 clock phases → accurate low-jitter phases from an injection-locked frequency divider

- Requirement trade-offs (conventional vs. multi-phase):
  - good device matching → accurate low-jitter clock generation
  - large device dimensions (older CMOS) → fast-switching transistors (modern CMOS)

Low-Jitter Clock Generation

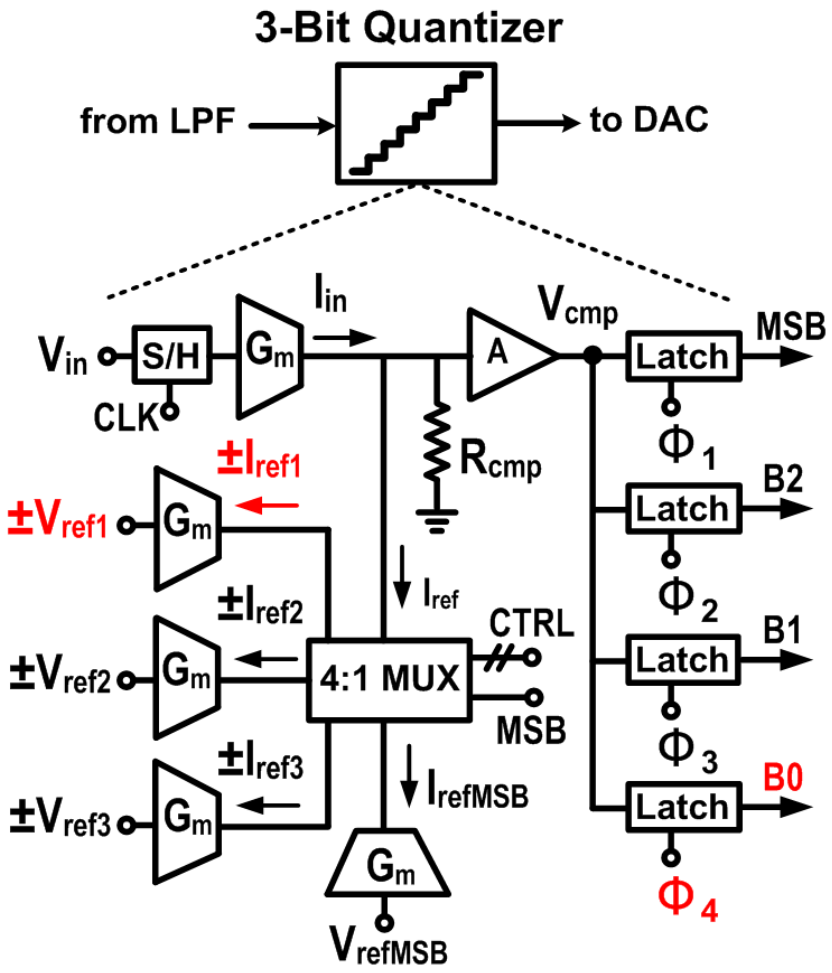


- Generation of 7 low-jitter clock phases at 400MHz
  - 2.8GHz inductor-capacitor (LC) tank voltage-controlled oscillator (VCO)
    - Improves phase noise (jitter) of the locked ring oscillator
  - Ring oscillator output phases control the timing of the quantizer & DAC logic circuits

Y.-C. Lo, H.-P. Chen, J. Silva-Martinez, and S. Hoyos, "A 1.8V, sub-mW, over 100% locking range, divide-by-3 and 7 complementary-injection-locked 4 GHz frequency divider," in *Proc. IEEE Custom Integrated Circuits Conf. (CICC)*, pp. 259-262, Sep. 2009.

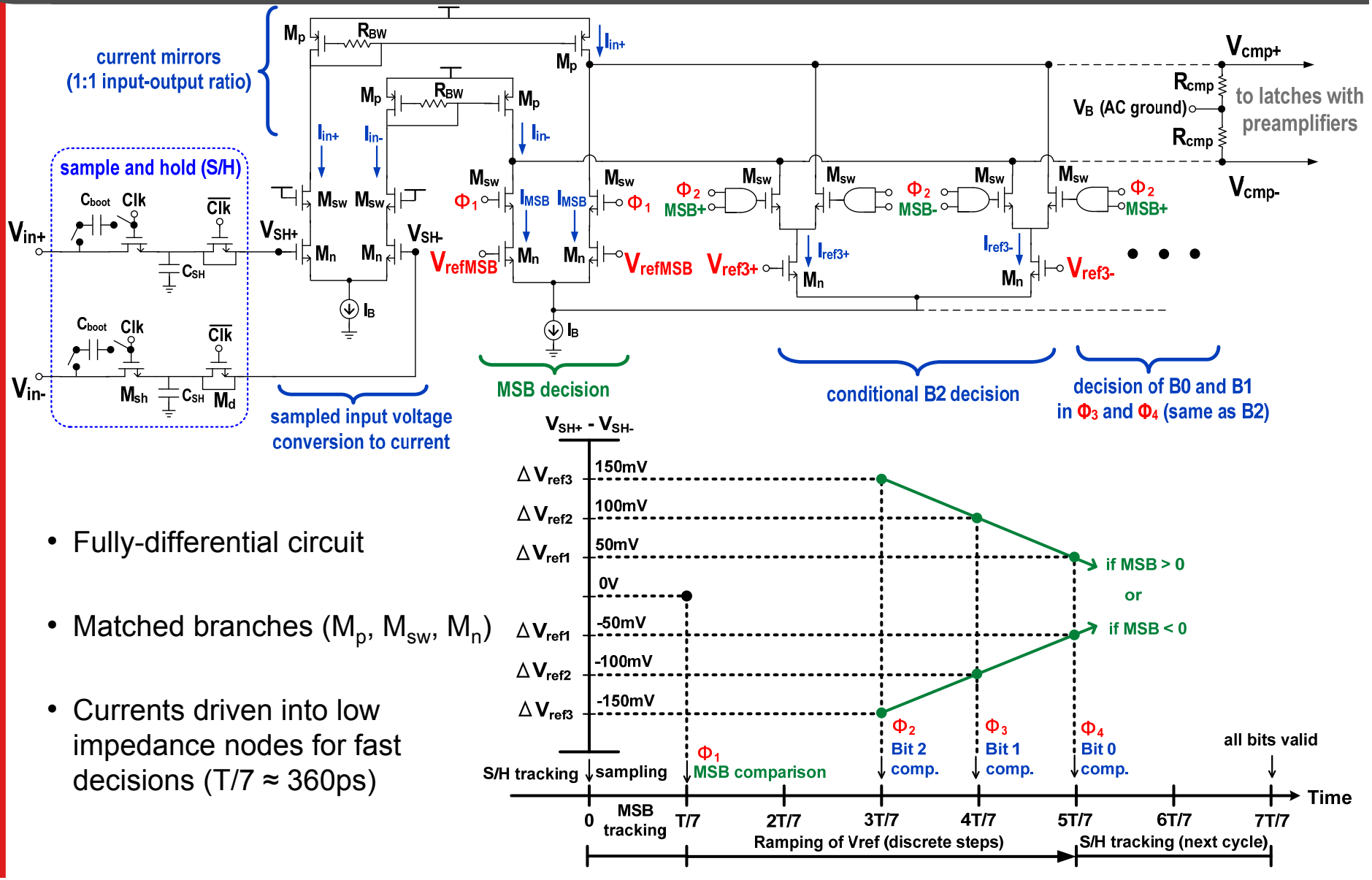
3-Bit Successive Approximation Quantizer

- 2-step current-mode quantization
  - 1st: Most significant bit (MSB) decision
  - 2nd: Successive comparisons of the sampled input with three reference levels
- Clocking
  - Sampling at 400MHz
  - Timing signals derived from the 7-phase clock generation for the DAC
- Current-mode comparison
  - Matched transconductors (G_m)
  - Reference currents are switched and compared to I_{in}
  - Fast low-voltage differential signaling configuration (R_{cmp} < 500Ω)
  - Ref. voltages can be un-buffered (a low source output impedance is not required)



Simplified single-ended equivalent circuit

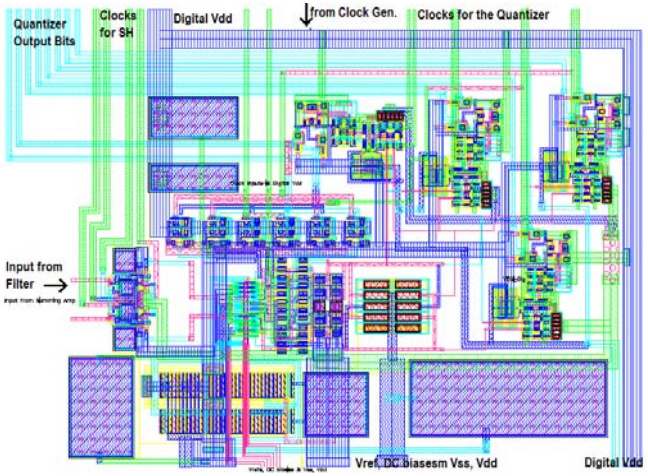
Quantizer Operation

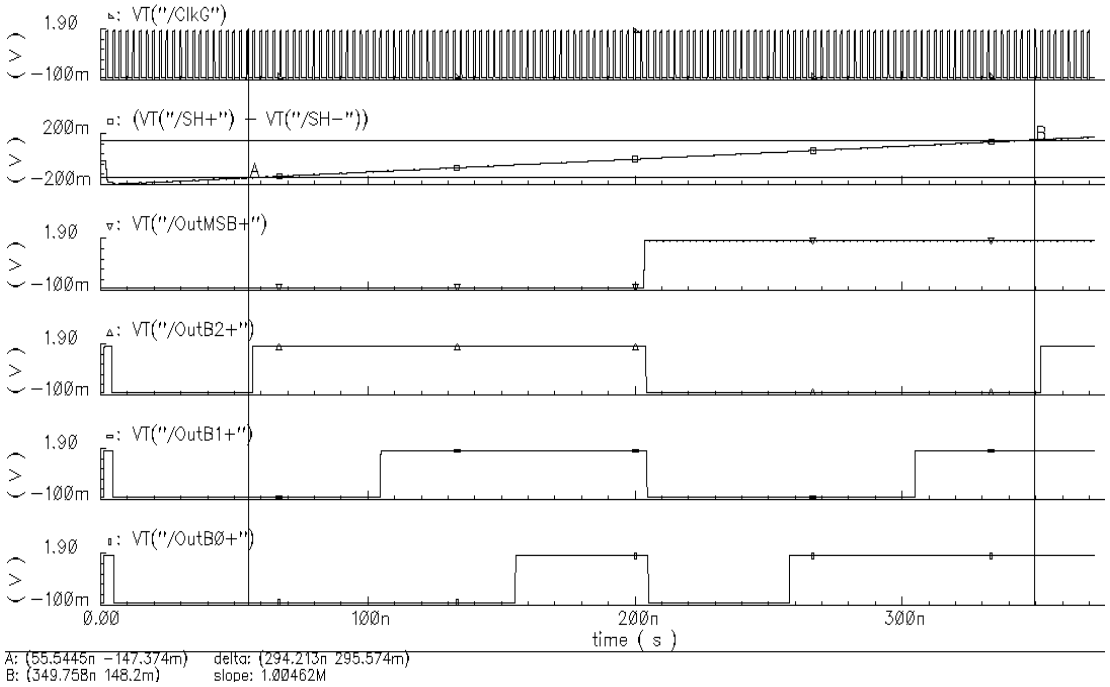


- Fully-differential circuit
- Matched branches (M_p, M_{sw}, M_n)
- Currents driven into low impedance nodes for fast decisions (T/7 ≈ 360ps)

Quantizer Simulations

- Implementation in 0.18µm CMOS with 1.8V supply
  - 24mW power consumption
  - 5mV resolution
  - Tunability to allow for PVT variations
    - Quantization levels can be shifted up to 30mV
    - Reference voltages are not in the direct signal path
  - Layout area of quantizer & timing circuitry: 750µm x 520 µm →





Ramp test: output bits for -200mV < V_{in} < 200mV

Differential Input	MSB	B2	B1	B0
150mV to 200mV	1	1	1	1
100mV to 150mV	1	0	1	1
50mV to 100mV	1	0	0	1
0 to 50mV	1	0	0	0
-50mV to 0	0	1	1	1
-100mV to -50mV	0	1	1	0
-150mV to -100mV	0	1	0	0
-200mV to -150mV	0	0	0	0

CT ΣΔ Modulators: State of the Art

	[A]	[B]	[C]	[D]	[E]	[F]	[G]	This Work
Peak SNDR	72dB	82dB	60dB	69dB	70dB	74dB	78.1dB	**67.7dB**
Bandwidth	10MHz	10MHz	20MHz	20MHz	20MHz	20MHz	20MHz	**25MHz**
Power Consumption	40mW	100mW	10.5mW	56mW	28mW	20mW	87mW	**48mW**
Sampling Frequency	950MHz	640MHz	250MHz	340MHz	420MHz	640MHz	900MHz	**400MHz**
Technology	130nm CMOS	180nm CMOS	65nm CMOS	90nm CMOS	90nm CMOS	130nm CMOS	130nm CMOS	**180nm CMOS**

[A] M. Z. Straayer and M. H. Perrott, "A 12-bit, 10-MHz bandwidth, continuous-time ΣΔ ADC with a 5-bit, 950-MS/s VCO-based quantizer," *IEEE J. Solid-State Circuits*, vol. 43, no. 4, pp. 805-814, Apr. 2008.

[B] W. Yang, W. Schofield, H. Shibata, S. Korrapati, A. Shaikh, N. Abaskharoun, and D. Ribner, "A 100mW 10MHz-BW CT ΔΣ modulator with 87dB DR and 91dBc IMD," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, pp. 498-631, Feb. 2008.

[C] V. Dhanasekaran, M. Gambhir, M. M. Elsayed, E. Sanchez-Sinencio, J. Silva-Martinez, C. Mishra, L. Chen, and E. Pankratz, "A 20MHz BW 68dB DR CT ΔΣ ADC based on a multi-bit time-domain quantizer and feedback element," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, pp. 174-175, Feb. 2009.

[D] L. J. Breems, R. Rutten, R. van Veldhoven, G. van der Weide, and H. Termeer, "A 56mW CT quadrature cascaded ΣΔ modulator with 77dB DR in a near zero-IF 20MHz band," *in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, pp. 238-239, Feb. 2007.

[E] P. Malla, H. Lakdawala, K. Kornegay, and K. Soumyanath, "A 28mW spectrum-sensing reconfigurable 20MHz 72dB-SNR 70dB-SNDR DT ΔΣ ADC for 802.11n/WiMAX Receivers," *in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, pp. 496-497, Feb. 2008.

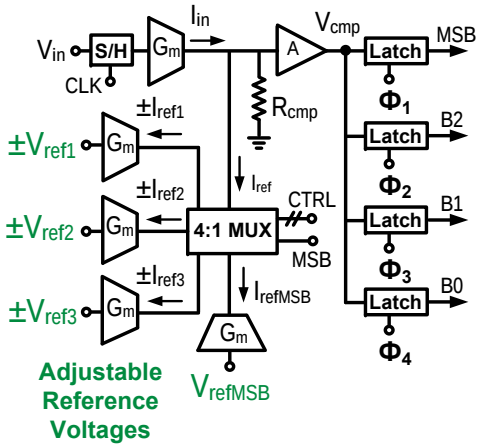
[F] G. Mitteregger, C. Ebner, S. Mechnig, T. Blon, C. Holuigue, and E. Romani, "A 20-mW 640-MHz CMOS continuous-time ΣΔ ADC with 20-MHz signal bandwidth, 80-dB dynamic range and 12-bit ENOB," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2641-2649, Dec. 2006.

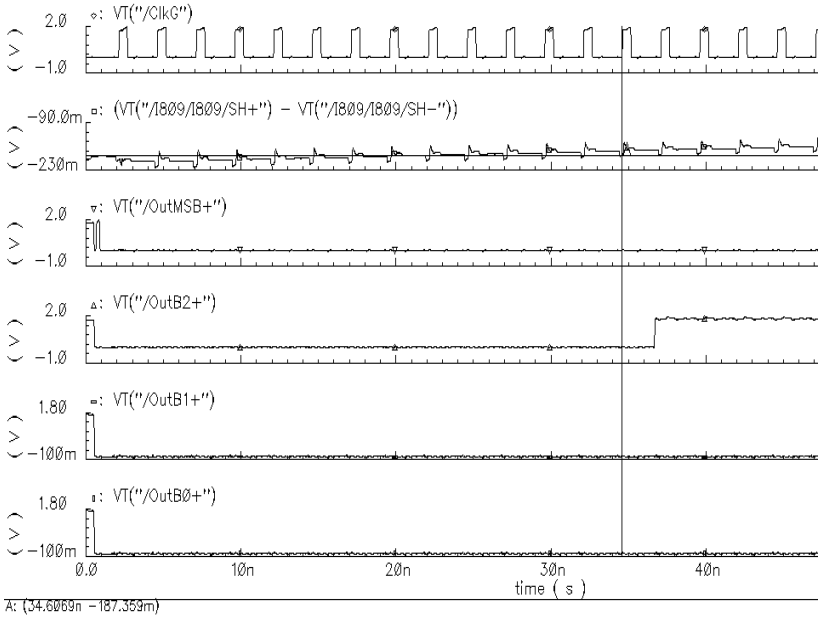
[G] M. Park and M. Perrott, "A 0.13μm CMOS 78dB SNDR 87mW 20MHz BW CT ΔΣ ADC with VCO-based integrator and quantizer," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, pp. 170-171, 171a, Feb. 2009.

Quantizer: Process Variation Compensation

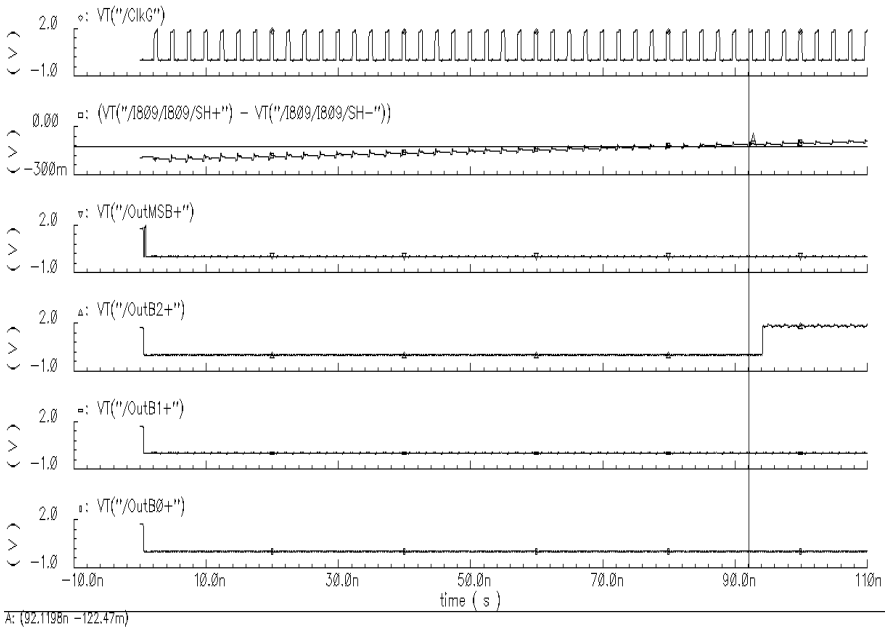
- Adjustable reference voltages
  - Quantization levels can be shifted up to 30mV
  - Do not have to be buffered
    (current-mode comparison → ref. voltages not in direct signal path)

- Example: shift of quantization level for bit 2
  - Schematic simulation with modeled pad/package parasitics
  - Nominal: transition at -153.6mV with V_{ref3} = 150mV





Bit transition at -187.4mV with V_{ref3} = 180mV



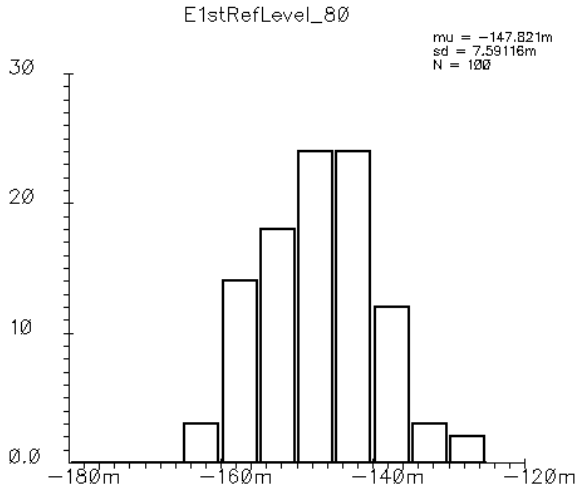
Bit transition at -122.5mV with V_{ref3} = 120mV

Quantizer: Technology Scaling & Process Variation

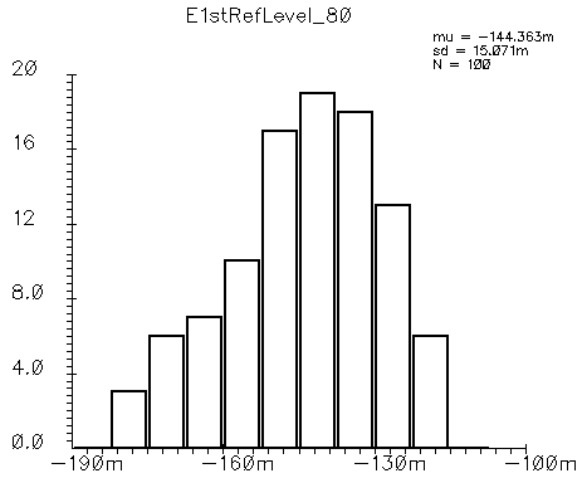
Key quantizer performance differences due to design scaling:

	Jazz 0.18µm CMOS	UMC 90nm CMOS
Resolution (nominal corner, no jitter)	**+/-5mV**	**+/-7mV**
Static power: quantizer core	**6.8mW**	**0.5mW**
Static power: diff. amp. & latch	**4 x 4.3mW**	**4 x 0.3mW**
Layout area	**750µm x 520µm** (actual area for core, logic, routing)	**estimate: ~500µm x 500µm** (~1/3 of active area, but similar passive device sizes & routing)
Clock frequency (7 phases with equal spacing and 50% duty cycle)	**400MHz**	**400MHz**

Histograms of the 1st reference level (-150mV) from Monte Carlo simulations with 100 runs:



0.18µm CMOS



90nm CMOS

Quantizer: Summary & Conclusions

- Functionality verified through measurements
  - Quantizer operated within a ΣΔ ADC prototype (0.18μm CMOS technology)
- Quantization with multi-phase clocks provides a viable alternative to typical flash quantizers in ΣΔ modulators
  - Optimized for combination with a single-element PWM DAC that avoids unit element mismatch problems due to process variations
  - Benefits from fast-switching transistors in modern CMOS technologies
    - For the same specifications: power of 90nm design < 10% power of 0.18μm design
- Tuning "knobs" are available to compensate for PVT variations
  - Quantization levels can be shifted individually via reference voltage adjustments
- A low-jitter clock source is mandatory
  - < 50ps RMS period jitter is required for the standalone 3-bit quantizer operation

C.-Y. Lu, M. Onabajo, V. Gadde, Y.-C. Lo, H.-P. Chen, V. Periasamy, and J. Silva-Martinez, "A 25MHz bandwidth 5th-order continuous-time lowpass sigma-delta modulator with 67.7dB SNDR using time-domain quantization and feedback," *IEEE J. Solid-State Circuits*, vol. 45, no. 9, pp. 1795-1808, Sept. 2010.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